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Integration of Next Generation Critical Infrastructure Sensor Technologies

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1.0 Project Description

This project is focused on advancing current protective relaying and control through verifying next generation timing systems and sensors with current commercial off the shelf protective relays. This will further research in the field of advanced grid modernization and demonstrate interoperability between next-generation protective relays and voltage and current sensors. These commercial off the shelf (COTS) technologies were tested and integrated with next generation sensor technologies, with the results documented below.

2.0 Next Generation Sensor Evaluation

Novel, highly advanced voltage and current sensors are being developed nation-wide, and their interoperability with COTS protective relaying equipment is paramount to the viability of their deployment onto the electrical grid. Savannah River National Lab (SRNL) has proposed to test one of these next generation sensors purchased through previous lab-directed research and development (LDRD) projects, which is currently installed in the High Current Calibration Laboratory at SRNL. This system is a fiber optic voltage and current sensor that SRNL previously tested at the Clemson eGRID facility.

The difficulty with integrating fiber optic sensors with COTS protective relays lies with the current standard for power sensor outputs. Traditionally, protective relays are design to measure currents and voltages with magnetic core current transformers (CT) and potential transformers (PT), who's output which can range from 1-5 amps for the CT, or range from 120-400 volts for the PT. Next generation sensors are not equipped to output these types of analog ranges and COTS devices are not established to receive digital data from fiber optic sensors without modification. Therefore, an integration method is studied in this report to test the capability of bypassing the traditional CT/PT inputs on state-of-the-art COTS protective relays and configuring them to receive data on their low voltage test ports, which is compatible with the voltage levels produced by a fiber optic sensor. This method of connecting fiber optic sensors also requires the determination of associated signal gains and relay configurations necessary for accurate operation.

2.1 Low Level Interface Testing Equipment

The experiments performed to develop and verify this capability were all performed in the Savannah River National Lab Critical Infrastructure and Industrial Control System Cyber Security Lab (S-CIIC). This lab consists of, among other things, a wide variety of Schweitzer Engineering Laboratory protective relays with associated networking equipment such as ethernet gateways, managed switches, and a GPS timing module to receive and distribute a common, highly accurate timing signal. This lab's purpose is to emulate a multitude of critical infrastructure protective equipment networks for hardware-in-the-loop (HIL) testing and for industrial network cyber security research and development. Included in the lab equipment listing is a Real Time Digital Simulator (RTDS) HIL system that can emulate low-level analog and digital signals that are specified and designed in a Real-time Simulation Computer Aided Design (RSCAD) power grid simulation, which is also built in the lab.

A small network of engineering control stations and human machine interfaces (HMIs) are also included in the lab to emulate Purdue level 2 and 3 devices that are commonly found in critical infrastructure networks. These workstations are used to program and interface with all networked equipment, as well as act as HMI and engineering workstations during experiments. A diagram showing the equipment used during these experiments in the S-CIIC is shown below.

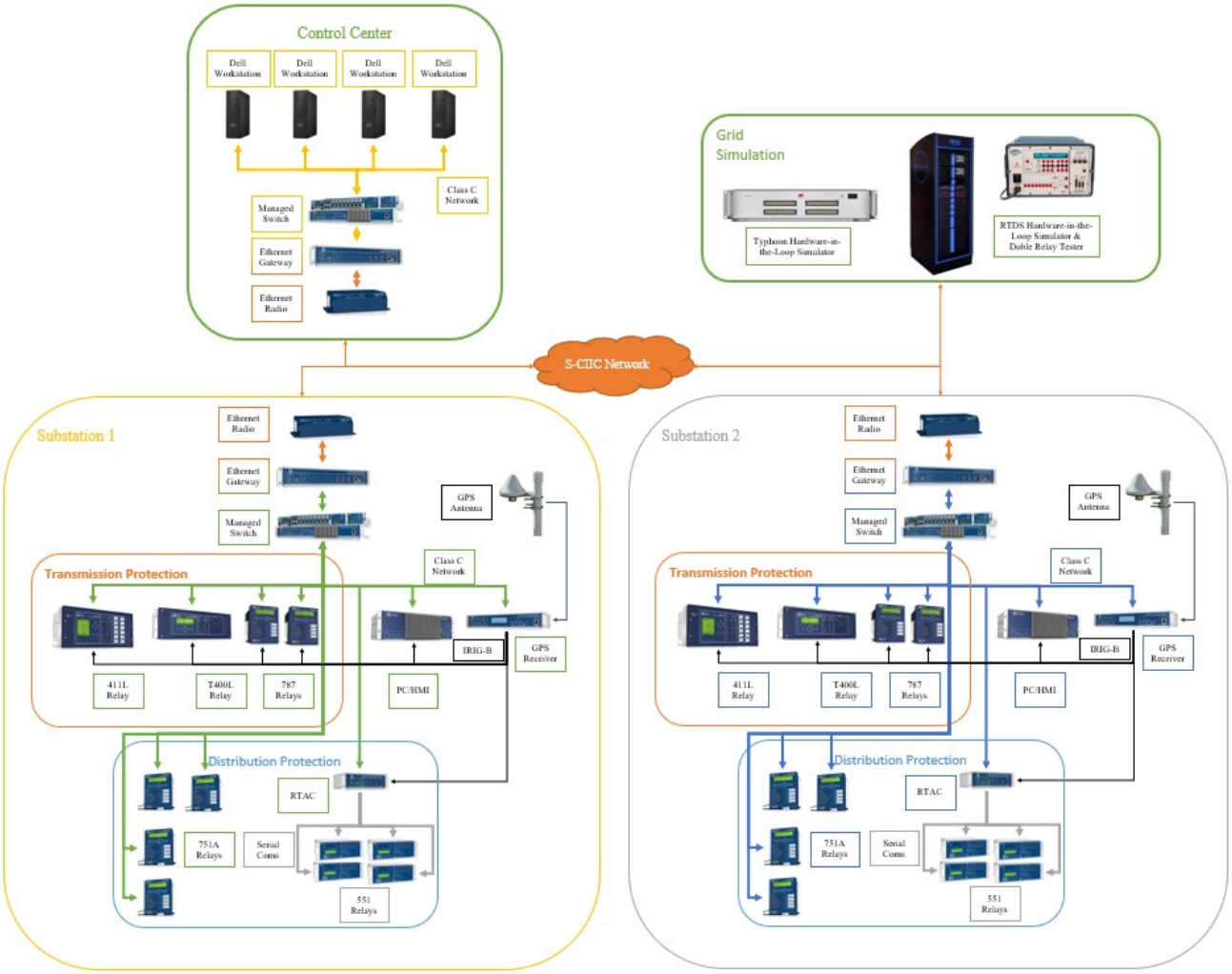

Figure 2-1. Partial S-CIIC Equipment Network Diagram

2.2 Low Level Interface Testing Methodology

The primary objective in testing the relays shown in Figure 2-1 is to form a methodology for upgrading the hardware capabilities of a variety of Schweitzer relays to accept low-level voltage signals. This process requires physically altering the relay in order to access the low-level input interface that is normally not accessible. Most of the Schweitzer relays that were tested in this experiment had the capability to accept low-level inputs, but with minor hardware modifications. The methodology developed to interface with the low-level inputs for each Schweitzer relay is detailed in the results and discussion section below.

Once the low-level inputs were accessed, the performance of the inputs were tested and quantified using the RTDS hardware-in-the-loop simulator to emulate low level signals produced by next generation fiber optic CT/PT sensors. The RTDS system includes a high-performance NovaCor processing board along with a variety of analog and digital input/output cards used to link the simulation to the hardware under test. In order to produce realistic low-level signals, a power grid simulation was developed using the RSCAD software. For this experiment, the power grid model developed was the Savannah River Site (SRS) 115kV transmission grid. This model is a thirty-seven-bus system with three ties to the local energy provider which is modeled as a source for each tie-in. Each of the transmission lines have also been accurately modeled in the simulation, with loads at each of the load buses modeled as steady state loads for simplicity. The one-line diagram of the simulation is shown below.

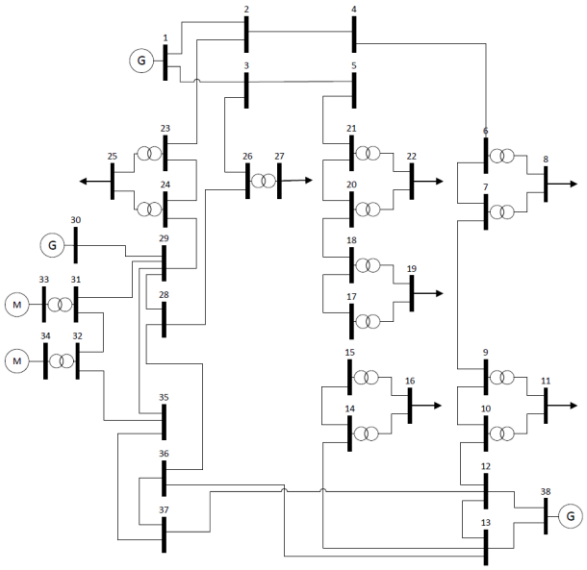

Figure 2-2. SRS 115kV One Line Diagram

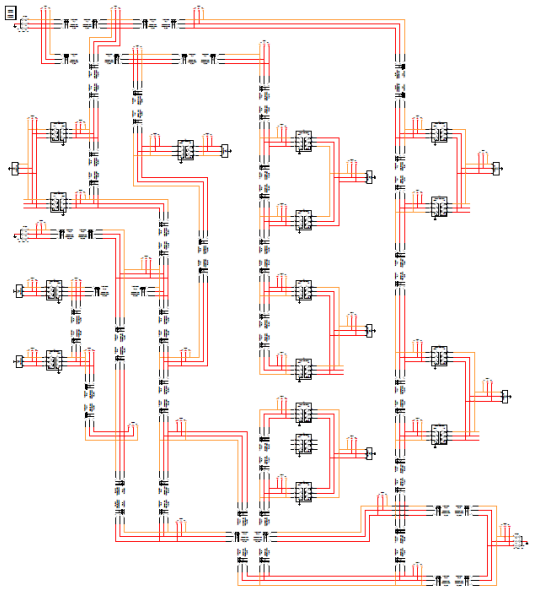

Figure 2-3. SRS 115kV Grid Modeled in RSCAD

In order to emulate next-generation CT/PT signals for the hardware-in-the-loop testing, voltage and current signals were selected from a bus to be converted from digital to analog signals within the simulation, and then sent from an analog output card in the RTDS to the low-level interface within the hardware under test. The voltage and current signals outputted from the RTDS have the capability to range from -10v to +10v, however the hardware under test often times has a much smaller range of voltages that the low-level inputs can accept. To combat this problem and protect the hardware under test, the gain of the outbound RTDS signal is altered in the RSCAD software to maintain a signal voltage level that will not damage the hardware. Generally, for the Schweitzer relays under test in these experiments, the maximum acceptable voltage level that the low-level inputs can accept is 6.6v peak-to-peak, meaning for an AC signal, the maximum amplitude of the waveform from the RTDS must not exceed 3.3v.

In order to accurately represent the signals, inbound from the RTDS system to the Schweitzer hardware under test, the gain was calculated with the correct relationship between the RTDS signal voltage (0-3.3v) and the expected voltage values from the simulation, which in this case was in the 115kV range. The calculated gain was inputted into the Schweitzer relays via the AcSELerator software. To test and verify the accuracy of the gains that were selected and calculated in both the RTDS system and the Schweitzer hardware, the simulation runtime in RSCAD was initiated, and then the real-time bus values in the

simulation were compared to the real-time voltage and current values on the Schweitzer relays. The section below documents the methodologies for each of the relays under test, along with the results of each trial.

3.0 Results and Discussion

The following section will detail the process to connect to the low-level interfaces for each of the relays that were a part of this study. Each relay had differences due to the variety of applications that they are subjected to, but the underlying process was mostly the same: find the cable harness or pin header that is responsible for transporting low-level signals from the measurement hardware to the main board and use that interface to inject low-level signals. The low-level signal interface serves as the connection point for analog signals from the RTDS system, as well as analog signals from next-generation sensor technologies that output low-level signals.

3.1 SEL-411L Differential Protection Relay

The SEL-411L relay is a high-speed transmission line differential, distance, and current protection relay that has reclosing, synchronism check, circuit breaker failure protection, and series compensated line protection logic among a multitude of other protection functions. This relay is primarily used for long lengths of transmission line or cable where differential protection is preferred.

In order to access and interface with the low-level inputs, the relay front-facing panel must be removed. Taking the front panel off reveals two boards, the relay main board is located on top, whereas the input module board is located on the bottom. The relay main board contains a processing module that accepts inputs from the input module board via a 34-pin connector on the right side of the assembly. This 34-pin ribbon cable is responsible for transporting low-level signals from the input module board to the relay main board. The cable can be removed from the relay main board and can be replaced with a custom test cable with the signals specified in the diagram below.

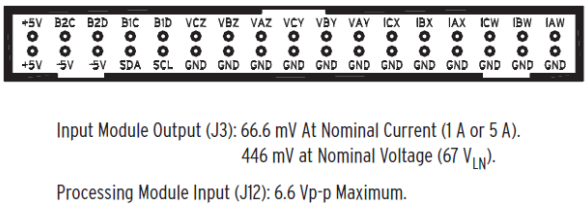

Figure 3-1. SEL-411L Ribbon Cable Signal Pinout

The signals shown in the diagram above include two three-phase currents (inputs W and X) and two three-phase voltages (inputs Y and Z) that can then be linked to an RSCAD simulation with a custom-built ribbon cable that then connects to the output pins of a RTDS GTAO card. It should be noted that the maximum rated voltage is listed in the figure above and should be strictly adhered to in order to avoid hardware damage.

3.2 SEL-T400L Traveling Wave Protection Relay

The SEL-T400L relay is an ultra-high-speed line protective relay for power transmission lines. Using state-of-the-art protection scheme techniques such as traveling waves and incremental quantities, the SEL-T400L has the capability to trip line faults in 2-5 ms depending on line length, fault characteristics, and system conditions. The SEL-T400L features very accurate traveling-wave fault locating techniques, high resolution time synchronized fault recording, and high-frequency power system event monitoring with a 1 MHz digital fault recorder. This relay is often found in large lengths of transmission line that require an extremely fast tripping time and large transient stability margins.

The low-level interface on the SEL-T400L can only be accessed by specifying that low-level input capability is required when ordering. Specifying low-level capability with a SEL-T400L adds additional coaxial ports on the back of the relay, which can then be connected to an RSCAD simulation via a GTAO card on an RTDS system.

3.3 SEL-787 Transformer Protection Relay

The SEL-787 relay is designed to protect transformers with as many as four windings/terminals via current differential, restricted earth fault, and overcurrent protection, among a variety of other protection functions. The 700 series relays are modular by design, using printed circuit board cards that can be installed easily for simple hardware upgrades and flexible ordering options. Due to the modularity of the 700 series, the low-level signal inputs will vary depending on the circuit board card installed. However, this means that the low-level signal inputs can be upgraded easily by ordering additional circuit board cards.

As previously stated, the low-level inputs vary based on the cards installed in the SEL-787. There are a total of 6 cards that host a low-level interface for analog current in (ACI) and analog voltage in (AVI). These cards include five options that fit into "Slot E" (6 ACI, 4 ACI/3 VI, 3 ACI/4 AVI, 1 ACI/3 AVI, 1ACI) and one option that fits into "Slot Z" (6 ACI) inside the relay. Each of the six options for the cards have a Connector "J2" that allows for connection to the low-level signal inputs, which is a fourteen-pin header. The J2 connector signal pinout for each module board is shown below.

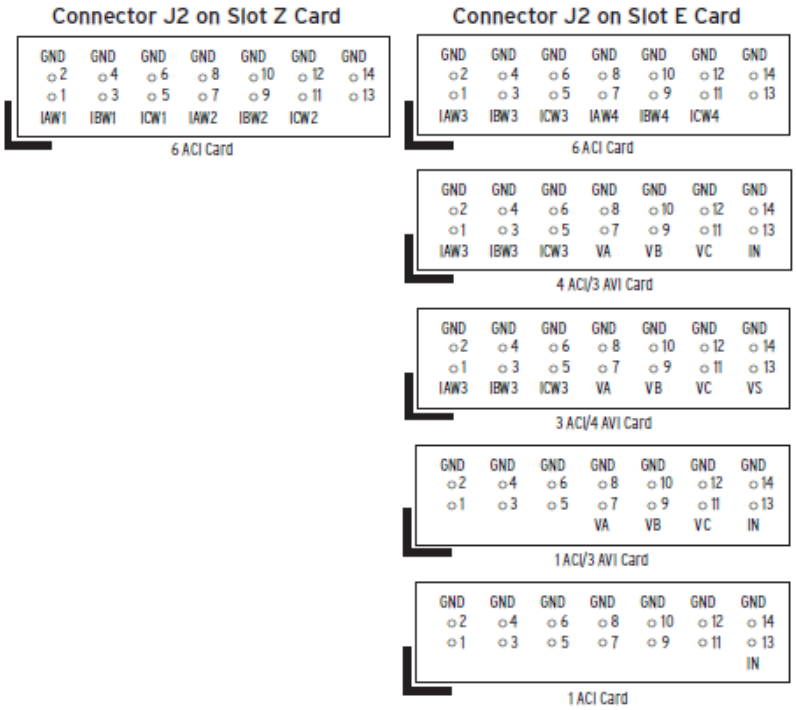

Figure 3-2. SEL-787 J2 Signal Pinout

The signals detailed above in each of the pinout diagrams depict varying levels of input capability. This ranges from three to four winding systems with neutral current measurements all the way to complete three-phase voltage measurement for RTDS connectivity. The next step in accessing the low-level interface for the SEL-787 after the J2 connectors have been identified is to adjust pin header jumpers appropriately. On the 6 ACI board in slot Z, jumpers JMP1-JMP6 shown in the figure below must be adjusted from pin 1-2 (normal position) to pin 2-3 (low-level test position). After the pins have been adjusted for the slot Z board, the J2 connector can be utilized by connecting a ribbon cable to it.

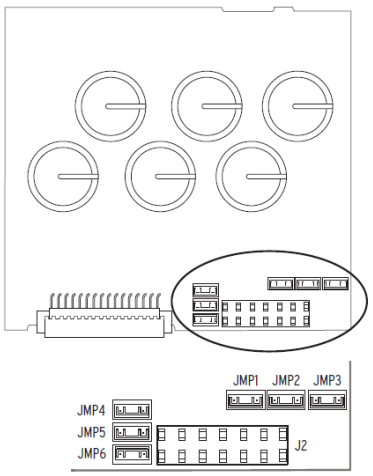

Figure 3-3. SEL-787 Jumper and J2 Connector Location on Slot Z Board

For the boards in slot E, the jumper location will vary depending on the type of board inserted. For the 6 ACI board, the jumpers JMP1-JMP6 shown in the figure above must be adjusted from pin 1-2 (normal position) to pin 2-3 (low-level test position). After the pins have been adjusted for the 6 ACI slot E board, the J2 connector can be utilized by connecting a ribbon cable to it. If the board in slot E has a 3 ACI/4AVI or 4 ACI/3 AVI instead of a 6 ACI card, then remove the board and locate the pins to move from CT_A to AMS_A, CT_B to AMS_B, and CT_C to AMS_C, shown in the figure below.

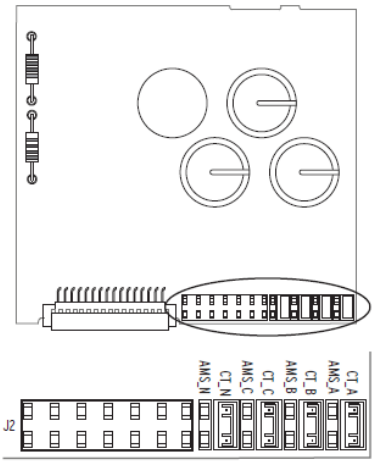

Figure 3-4. SEL-787 Jumper and J2 Connector Location on Slot E Board

Also, move the CT_N pin to the AMS_N pin for the 4 ACI/ 3AVI board. If slot E has a 1 ACI/3 AVI or 1 ACI card, move the CT_N pin to the AMS_N pin. After the pins have been adjusted for any of the above slot E boards, the J2 connector can be utilized by connecting a ribbon cable to it. It should be noted that the low-level input voltage levels are not specified for the SEL-751A, and so they should assume to be 6.2 V_{pp} maximum, as with other similar models of SEL relays.

3.4 SEL-751A Feeder Protection Relay

The SEL-751A relay is designed to provide overcurrent protection to various distribution components, including feeders, transformers, and other distribution level devices. The base model of the relay provides Phase, Ground, and Neutral instantaneous and time overcurrent protection among a variety of other overcurrent protection schemes. This model of relay is used widely in transformer protection and can be found in a wide variety of feeder applications. As with the SEL-787, the SEL-751A is from the 700 series relays, allowing for a flexible, modular design for simple ordering and upgrading options. Due to the modularity of the 700 series, the low-level signal inputs will vary depending on the circuit board installed.

As mentioned previously, the SEL-751A has multiple options for low-level signal input upgrades. In slot Z, there is one option of having the 4 ACI card, and in slot E there is the option of having either the 3 AVI card or the 3 AVI/4 AFDI card. The location of both slot E and slot Z is shown in the figure below. As with the SEL-787, the 4 ACI card in slot Z has a 14-pin male header for low-level signal interfacing labeled "J2". The 3 AVI and 3 AVI/4AFDI cards installed in slot E however have a 14-pin male header similar to the 4 ACI card in slot Z, but instead labeled "J3", and is located in a different section of the board. Both the J2 and J3 pin header would be connected to a ribbon cable, which could then interface with a low-level signal generator. The installation procedure into the relay is the exact same for any of the listed cards.

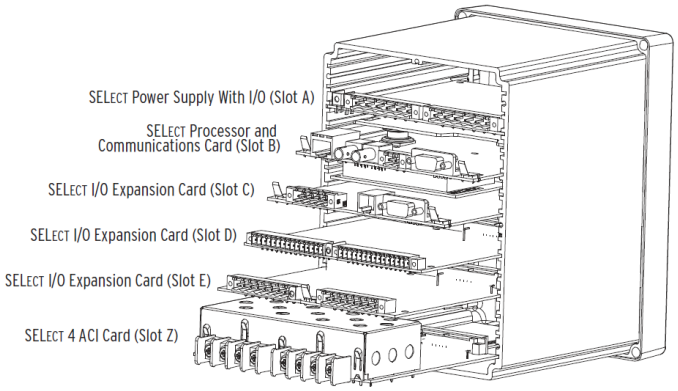

Figure 3-5. SEL-751A Slot Diagram

To install low-level compatible cards into the SEL-751A, the cards are simply slid into the respective card slots in either slot E or slot Z depending on which card is being installed. After the new cards have been installed, the relay is then powered on, with the message "STATUS FAIL, X Card Failure" on the screen. If this message is not on the screen, the card was inserted into the wrong slot. The remainder of the steps (detailed in the SEL-751A manual, "Section 2: Installation") to activate the card involves accepting the hardware change on the front panel screen and updating the part information within the device settings menu. After this has been done, a short reboot is performed by the device and the device is ready to accept low-level inputs. After the low-level inputs have been accessed, a ribbon cable connecting the inputs to a GTAO card in an RTDS system can be connected and low-level signals can be run. It should be noted that the low-level input voltage levels are not specified for the SEL-751A, and so they should assume to be 6.2 Vpp maximum, as with other similar models of SEL relays.

3.5 SEL-551 Overcurrent/Recloser Relay

The SEL-551 relay's primary function is the provide overcurrent protection and up to four shots of reclosing for faulted systems. There are numerous phase, ground, and negative-sequence overcurrent elements included with the overcurrent protection systems, as well as access to enhanced programmable protection schemes, demand metering, and sequential event recording among other capabilities. This relay is primarily found in utility distribution feeders, distribution buses, transformer banks, and other power system apparatuses.

In order to access and interface with the low-level signal inputs on the SEL-551, the relay front-facing panel must be removed. Taking the front panel off reveals two boards, the relay main board is located on top, whereas the input module board is located on the bottom. The relay main board contains a processing module that accepts inputs from the input module board via a 14-pin connector on the right side of the assembly. This 14-pin ribbon cable is responsible for transporting low-level signals from the input module board to the relay main board. The cable can be removed from the relay main board and can be replaced with a custom test cable with the signals specified in the diagram below.

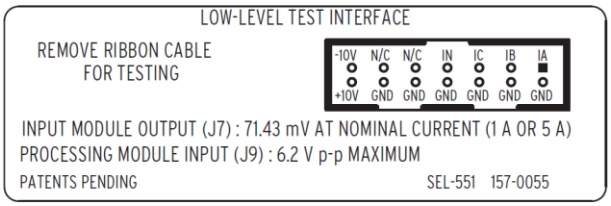

Figure 3-6. SEL-551 Ribbon Cable Low-Level Signal Pinout

The signals shown in the diagram above include one three-phase current with a neutral that can then be linked to an RSCAD simulation with a custom-built ribbon cable that then connects to the output pins of a RTDS GTAO card. It should be noted that the maximum rated voltage is listed in the figure above and should be strictly adhered to in order to avoid hardware damage.

3.6 SEL-351 Protection System

The SEL-351 Protection system is a synchrophasor-enabled relay that is ideal for directional overcurrent applications. This relay can be found in a wide variety of locations within a substation yard, with functions including transformer bank protection, transmission line protection and reclosing, utility distribution bus protection, and general utility distribution feeder protection and reclosing. There is a wide variety of ways to enable protection in these zones, utilizing overcurrent, harmonic blocking, voltage and synchronism check, frequency, and other power elements.

The SEL-351 comes with an easily accessible J12 connector on the main board, which is the output connector of the input module that connects the input module to the main board. This is accessed by simply removing the front panel of the relay. The location of the J12 connector is shown in the diagram below, with the 34 male pin header located on the right lower side of the main board.

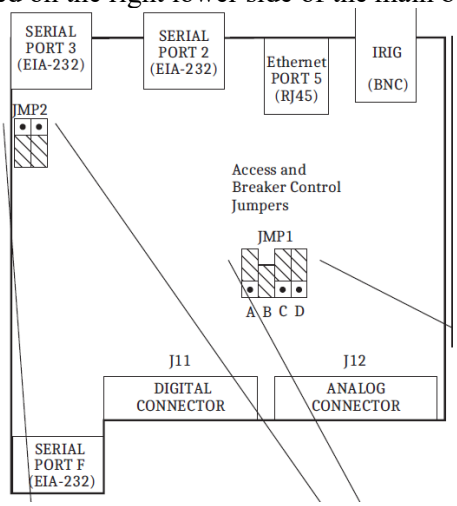

Figure 3-7. Location of J12 Connector on SEL-351 Main Board

After the J2 connector has been identified and located, the ribbon cable is removed to access the outputs of the input module (J2) and the inputs to the processing module (J12). The pinout diagram depicts the signals for each of the pins on the J12 connector.

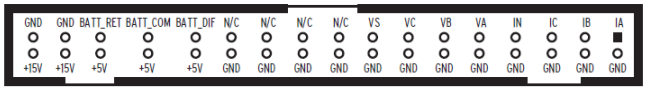

Figure 3-8. SEL-351 Ribbon Cable Low-Level Signal Pinout

As shown above, the signals for the pins on the J12 connector on the main board include a three-phase voltage, current, and other various battery monitoring pins. All of these pins have the capability of being connected to an RSCAD simulation via a GTAO card connected to an RTDS. It should be noted that the rated input voltage levels for this low-level signal interface is much higher than the previous models discussed, with the maximum allowable input voltage at 9 V_{pp}.