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SOLID-STATE DC AMPLIFIER WITH HIGH INPUT IMPEDANCE

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SOLID-STATE DC AMPLIFIER WITH HIGH INPUT IMPEDANCE

by

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ABSTRACT

A solid-state operational amplifier with a field-effect transistor at the input was designed and tested. The amplifier has an input resistance greater than 5×10^{11} ohms and an input leakage current less than 10^{-12} ampere at room temperature. The amplifier is useful in nuclear instrumentation applications where it is necessary to measure very small signal currents.

CONTENTS

LIST OF TABLES AND FIGURES

SOLID-STATE DC AMPLIFIER WITH HIGH INPUT IMPEDANCE

INTRODUCTION

An amplifier with high input impedance is needed in many nuclear instrumentation applications such as electrometers, radiation detection devices, and reactor log n-period systems. For many years electrometer vacuum tubes were the only input elements that could meet this high impedance requirement. However with the development of the field-effect transistor (FET), which has an extremely high input impedance (10^{11} - 10^{18} ohms), solid-state electronics can now be designed for these applications.

The amplifier described in this report represents an initial step toward improving nuclear measurement and control techniques by using field-effect transistors (FETs) and all solid-state circuitry. A specific application for the amplifier is in a new solid-state log n-period system. The logarithmic amplifier in such a system usually provides on a single scale an indication of neutron flux over a range of seven to eight decades. The usual practice of logarithmic conversion of the signal current from the ion chamber neutron detector has been to use a reverse biased thermionic diode. However diodes generally do not have a logarithmic relationship over more than six to seven decades. Work by Gibbons and Horn of Stanford University[1] has shown that a silicon transistor connected as the feedback element of an operational amplifier can be made to exhibit an accurate logarithmic transfer response over a range of nine decades. It is planned to use the present amplifier for experiments in such circuitry.

SUMMARY

A solid-state DC amplifier was designed for use as an operational amplifier. The circuit uses a field-effect transistor (FET) as the input circuit element and differential transistor stages to provide an overall voltage gain of 2400 (68 db). The gain-bandwidth product is 100 kc, and the temperature drift between 20 and 32°C is 1 mv, referred to the input.

Tests on the amplifier showed that good performance can be obtained with an FET at the input. Input characteristics of the circuit are limited only by the parameters of the FET.

DISCUSSION

Preliminary Work

A type SU348 field-effect transistor (FET) was selected for the input circuit on the basis that it had the highest input impedance of any FET available at the time. Laboratory tests were conducted to verify the operating characteristics of the FET, and several circuits were tested. The FET has the unique feature that either a positive or negative gate-source temperature coefficient can be obtained, dependent on the bias conditions.[2] Accordingly, in the initial experiments an effort was made to bias the FET to obtain a zero temperature coefficient. This would be most desirable, but it was found to lead to undesirably high noise levels. In the final design the operating bias was selected for minimum noise since temperature compensation could be provided elsewhere in the circuit.

FET Input Circuit

The input circuit (Figure 1) consists of an FET source follower used to drive a PNP transistor, 2N2177. The circuit has a DC gain of approximately 1.25.

Measurement of the DC input impedance of a device with such a high impedance is difficult because of unavoidable stray leakage currents in the test setup; however, some measurements were made to approximate the value. Resistors of known value were inserted in series with the circuit input, and gain-frequency curves were plotted. The 3-db point on the bandwidth curve occurred when the AC impedance was equal to the series input resistor value. A simple calculation gave input capacitance. The frequency roll-off of the circuit without series input resistance was 150 kc. "Bootstrapping" the circuit (connecting C_{BS} as shown in Figure 1) decreased the effective input capacitance. The bootstrapping applied positive feedback to the FET drain, reducing the gate-drain capacitance. Gain-frequency curves with and without bootstrapping are shown on Figures 2 and 3.

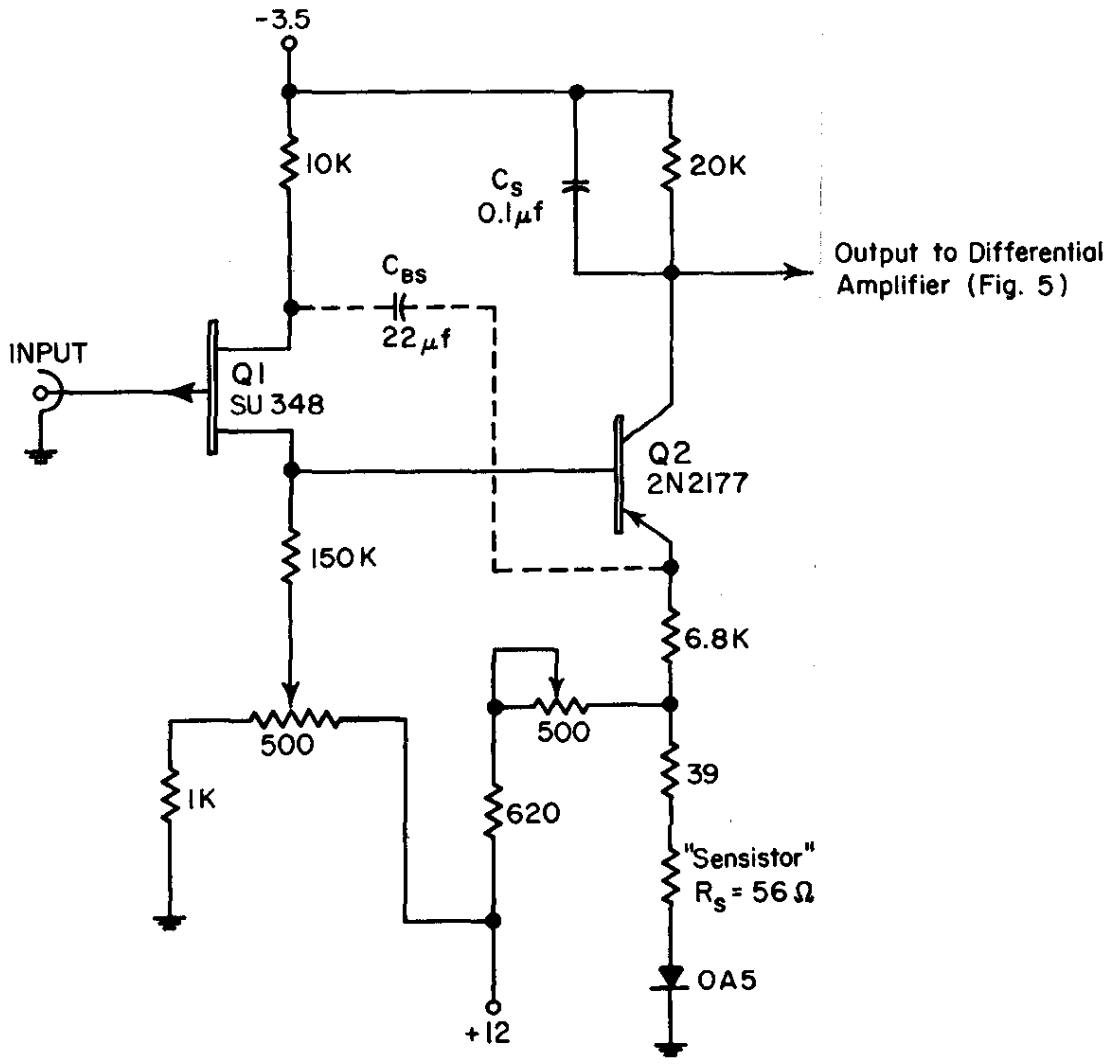


FIG. 1 FET INPUT CIRCUIT - SCHEMATIC

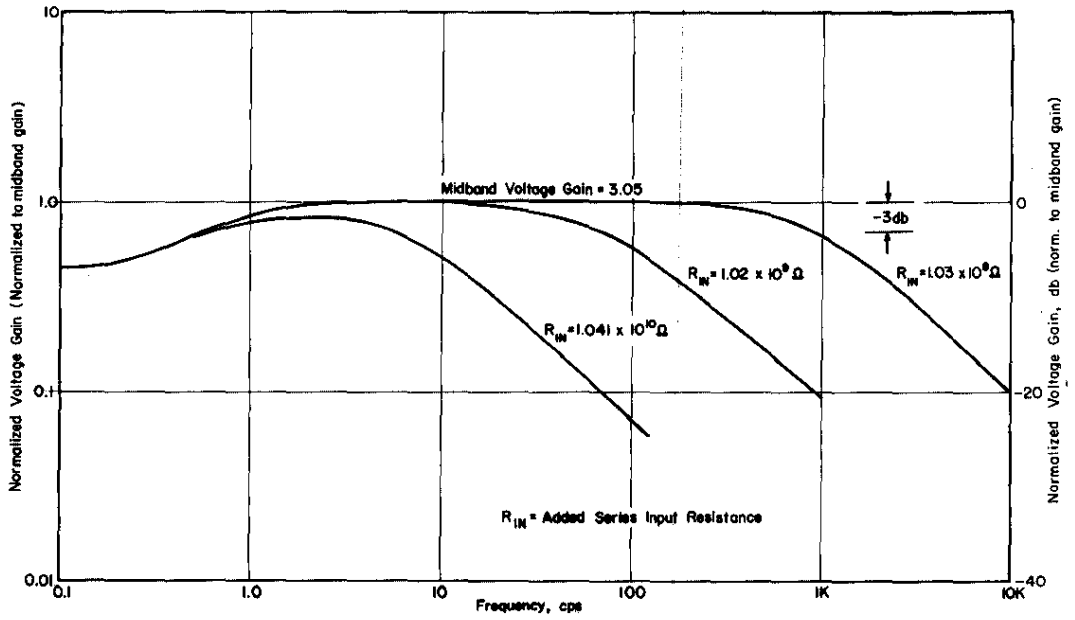


FIG. 2 BANDWIDTH CURVES - AMPLIFIER BOOTSTRAPPED

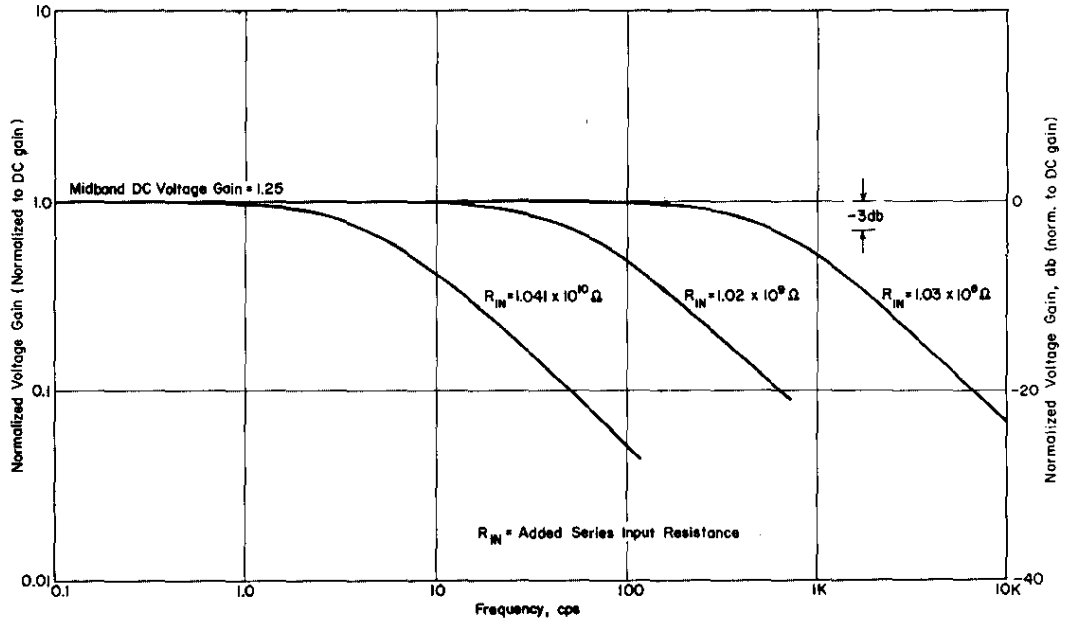


FIG. 3 BANDWIDTH CURVES - AMPLIFIER NOT BOOTSTRAPPED

The following values of input capacitance were calculated from the curves.

TABLE I

Input Capacitance Values

Circuit Conditions	AC Input Impedance, ohms	Frequency	Calculated Input Capacitance, pf
Bootstrapped	11.4×10^6	10 kc	1.4
	56.6×10^8	16.5 cps	1.7
Not Bootstrapped	11.4×10^6	6 kc	2.1
	56.6×10^8	11.5 cps	2.4

The DC input resistance was approximated using the same series input resistor method. When the value of series resistance approached the value of FET input resistance, the DC gain of the circuit was reduced. The data revealed that the input resistance was 500-1000 gigaohms (10^9 ohms).

Figure 4 shows the graphs of impedance vs. frequency. The final version of the operational amplifier tested in this report was not bootstrapped.

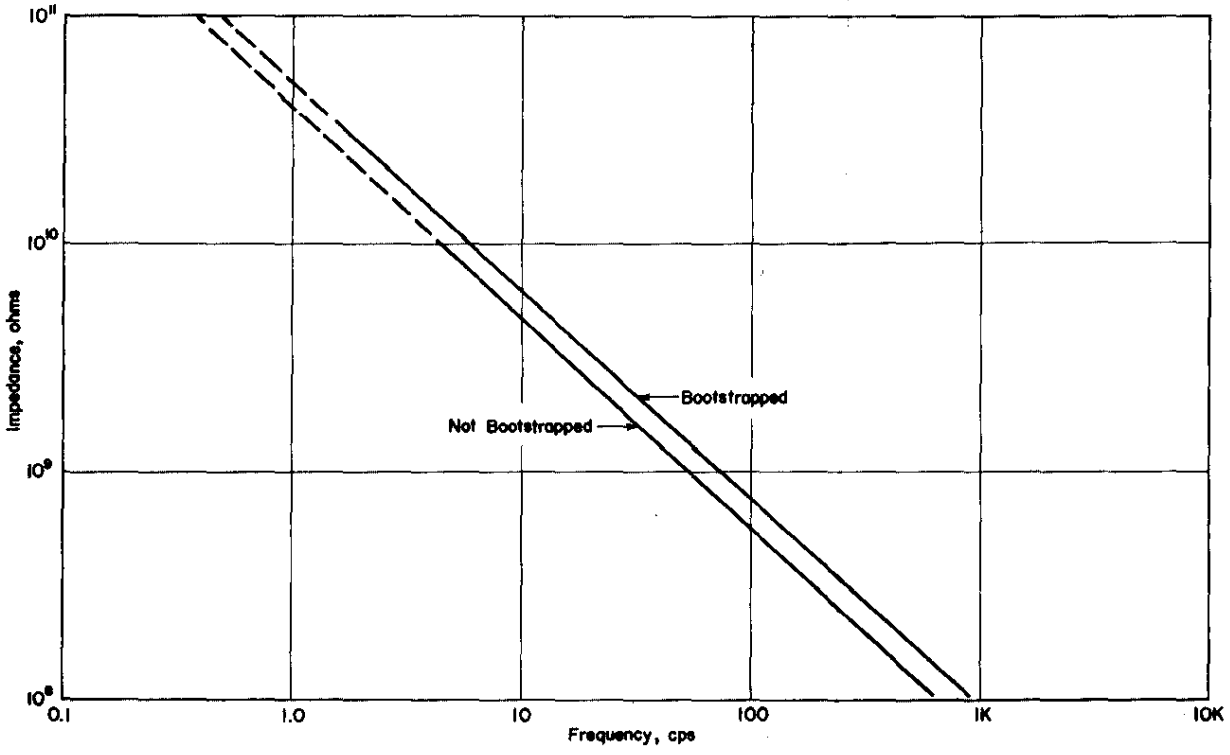


FIG. 4 IMPEDANCE VS. FREQUENCY - FET INPUT CIRCUITS

Differential Amplifier

The gain portion of the amplifier consists of three differential amplifier stages (Figure 5), with differential transistors for low drift. (A differential transistor consists of a matched pair of transistors constructed in a common can.) The overall differential DC gain was 3700. The roll-off frequency was 65 kc. The differential amplifier output has an overall temperature drift of 6 $\mu v/^{o}C$, referred to the input.

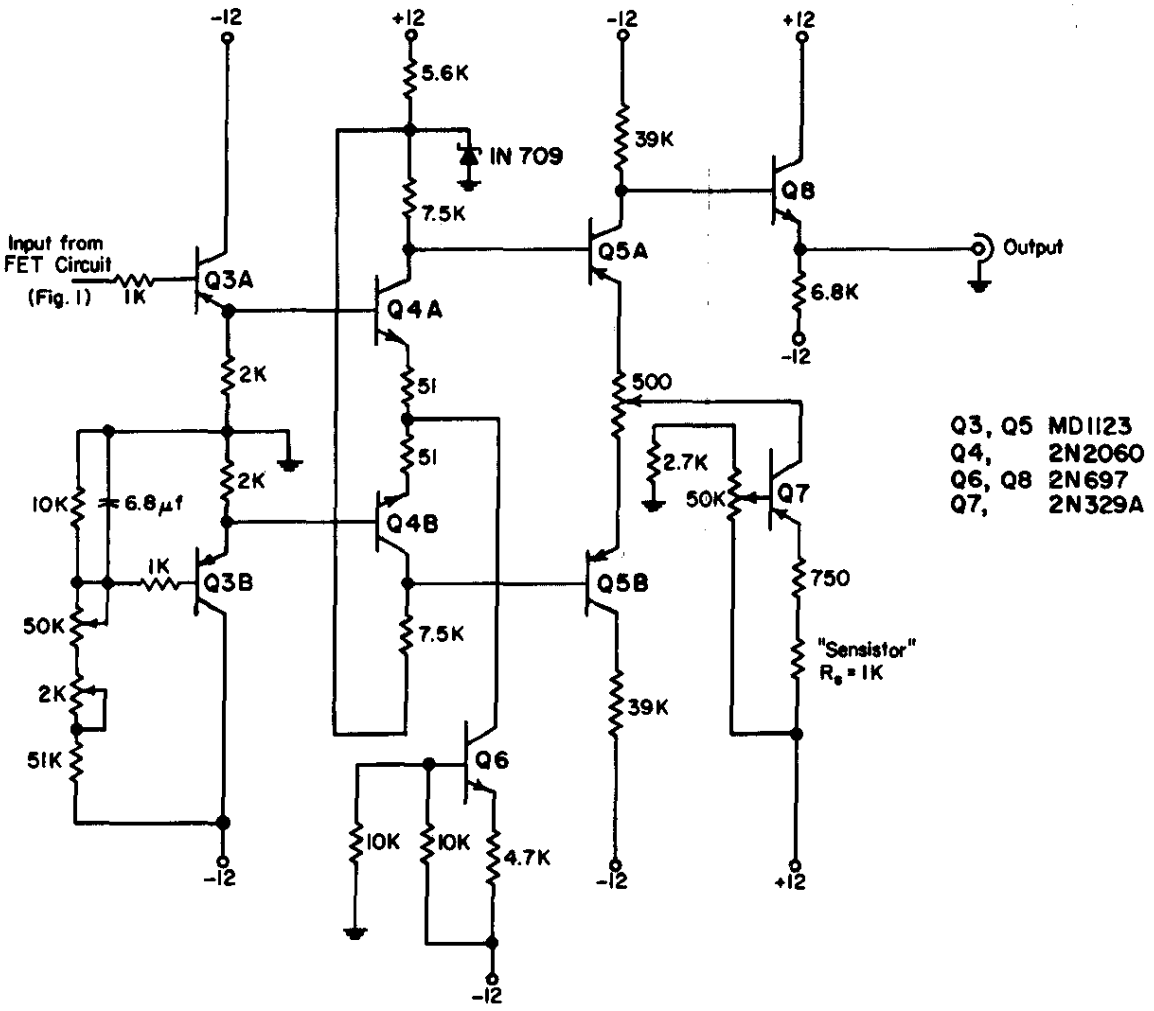


FIG. 5 DIFFERENTIAL AMPLIFIER - SCHEMATIC

Operational Amplifier

The integration of the FET input circuit and the differential gain stages (Figures 1 and 5) completes the operational amplifier. The open loop DC gain was 2400, rolling off at 60 kc. This resulted in an unstable closed loop operation since the gain was well above unity when 180° phase shift occurred in the amplifier; therefore, frequency shaping was applied in the FET circuit with a 0.1-μf capacitor across the 2N2177 load resistor (C_S, Figure 1). The amplifier was then stable with 100% negative feedback. Curves for open loop and closed loop conditions are shown in Figure 6. The circuit was cycled in a temperature test oven;

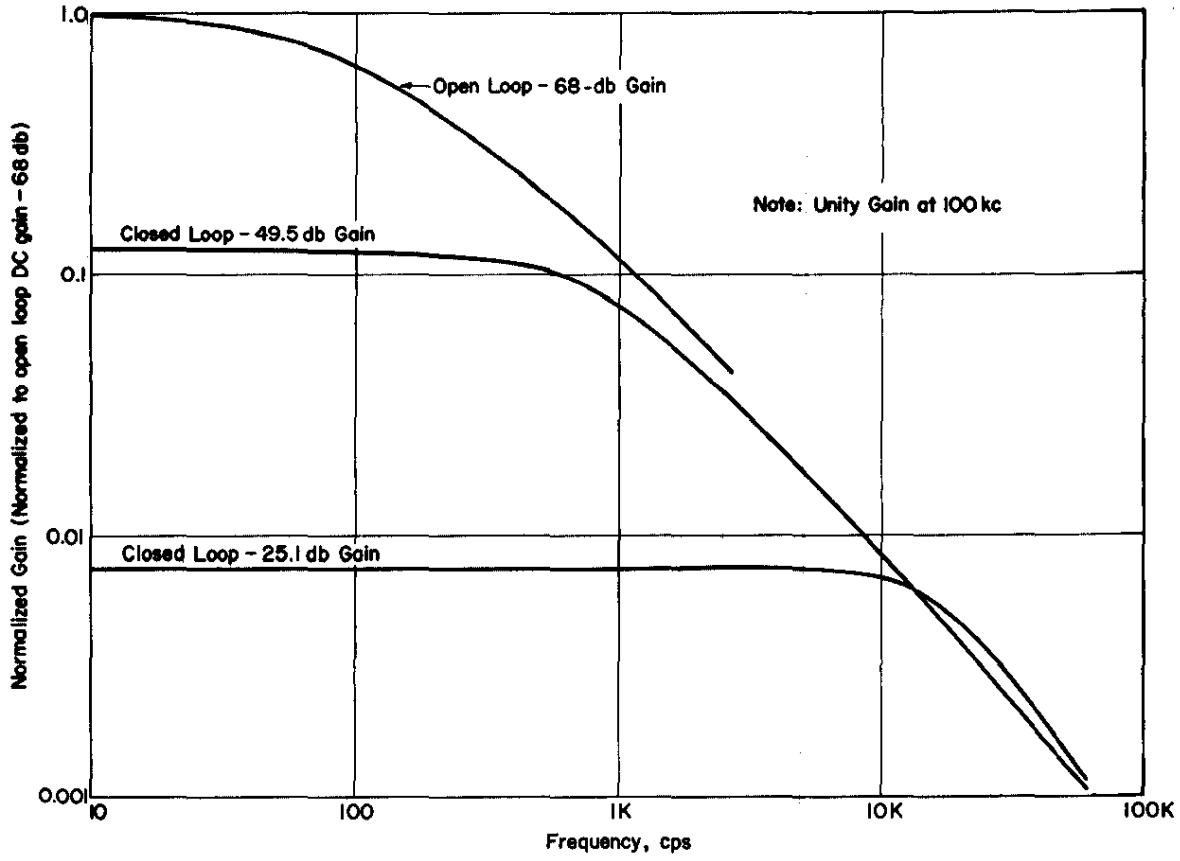


FIG. 6 GAIN - FREQUENCY CURVES - OPERATIONAL AMPLIFIER

total drift was 1 mv between 20 and 32°C, referred to the input, as shown in Figure 7. The overall performance of the amplifier is summarized in Table II. This performance is regarded as quite satisfactory for laboratory-type operation.

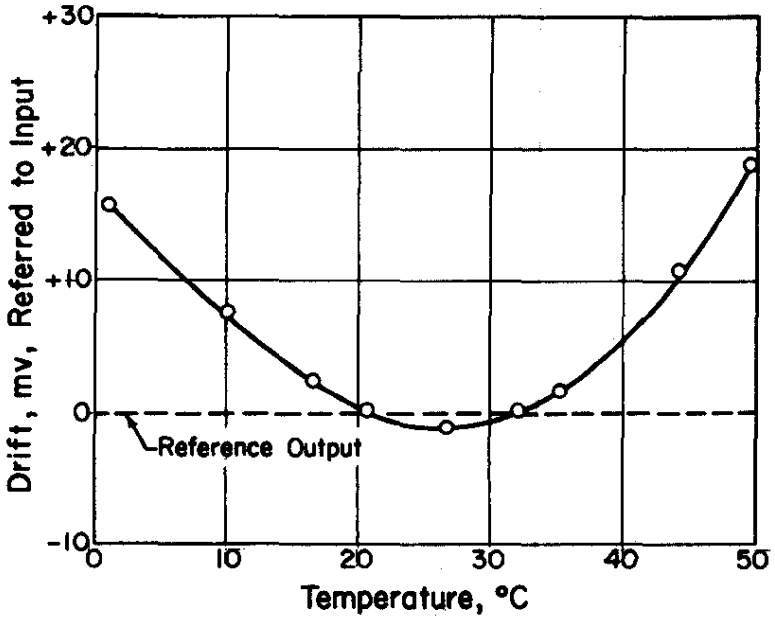


FIG. 7 VOLTAGE DRIFT OF OPERATIONAL AMPLIFIER

TABLE II

Operational Amplifier Specifications

DC voltage gain	2400 (68 db)
Bandwidth	100 kc
Input resistance	500 gigaohms
Input capacitance	2.3 pf
Output impedance	600 ohms
Output voltage	±1.5 volts
Input current	7×10^{-13} amp @ 23°C 5×10^{-12} amp @ 40°C
Voltage drift	1 mv total deviation referred to input between 20 and 32°C (Figure 7)
Warm-up drift	-50 mv in 3 hr at output
Output waveform rise time	3 ms

FUTURE WORK

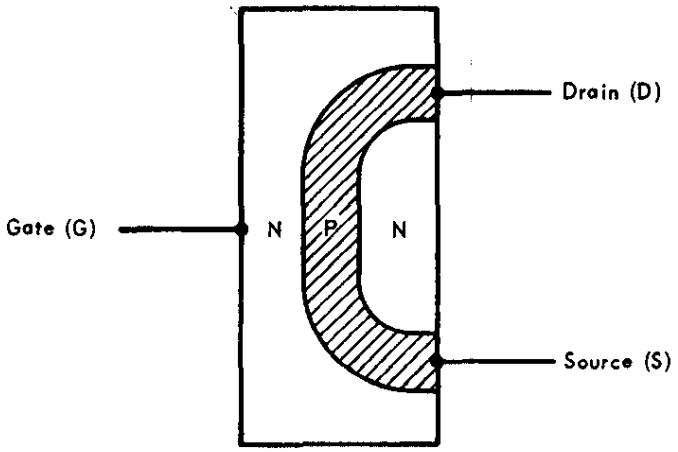
Since the start of this work a number of semiconductor manufacturers have introduced a metal oxide field-effect transistor (MOS FET), which uses an insulated gate and has a much higher input impedance than any other FET now available. Impedance ranges are 10^{15} - 10^{18} ohms. The development of the MOS FET is a breakthrough for solid-state circuit design. Immediate plans are to design an improved operational amplifier with MOS FETs and to use the new amplifier in a solid-state logarithmic converter circuit.

REFERENCES

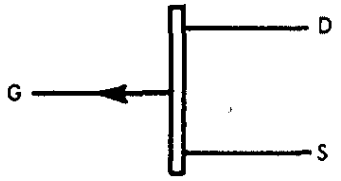
1. J. F. Gibbons and H. S. Horn. "A Circuit with Logarithmic Transfer Response Over 9 Decades." IEEE Transactions of the Circuit Theory Group, Volume CT-11, Number 3, September 1964.

2. "Biasing UNIFETs to Give Zero DC Drift." Application Note, Siliconix Incorporated, Sunnyvale, Calif., July 1963.

APPENDIX - FET DIAGRAMS



Simplified Construction Diagram



Circuit Symbol