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PAPER TAPE DATA ACQUISITION SYSTEM

R. J. SAND

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E. I. du Pont de Nemours & Co.
Savannah River Laboratory
Aiken, S. C. 29801

PREPARED FOR THE U. S. ENERGY RESEARCH AND DEVELOPMENT ADMINISTRATION UNDER CONTRACT AT(07-2)-1

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by

R. J. Sand

Approved by

D. E. Waters, Research Manager

Laboratory Operations and Services Division

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ABSTRACT

A system was developed to store chemical analysis data from scientific instruments. The data acquisition system stores, in dynamic memory, analog signals received from one to eight data channels. The channels are sampled at rates from 0.0025 Hz to 20 kHz. Data are later transferred to paper tape for subsequent analysis in a minicomputer.

CONTENTS

	Page
INTRODUCTION	5
PAPER TAPE DATA ACQUISITION SYSTEM	5
FUNCTION OF CIRCUITS	7
Timing Circuit	7
Data Acquisition Circuit	7
Data Input Circuit	8
Memory Circuit	8
Paper Tape Circuit	11

LIST OF FIGURES

No.		Page
1.	Logic Flow Chart	6
2.	Specimen of 8-Bit Paper Tape	7
3.	Logic Frame (Front View)	9
4.	Logic Frame (Rear View)	10
5.	Start-Stop Input TTL Wave Forms	11

PAPER TAPE DATA ACQUISITION SYSTEM

INTRODUCTION

A method was needed to record analog electrochemical instrument data for subsequent processing by minicomputer analysis programs. A wide range of data acquisition rates was required. Also desirable was the ability to sample various combinations of different input signals.

Basic equipment existed for data sampling, for rapid storage of data obtained at high rates, and for punching data on paper tape at low rates. Control electronics were designed and combined with existing equipment to produce a versatile data acquisition system. This system gathers data from any analog electrical signal at the presently available rates.

PAPER TAPE DATA ACQUISITION SYSTEM

The paper tape data acquisition system can sample up to eight analog channels at up to 20 kHz and can store data for as many as 512 samples in memory for later transfer to punched paper tape. The system uses a *Datel* DAS-16 multiplexing analog-to-digital converter (Datel Systems, Inc., Canton, Massachusetts), which may be expanded to 16 analog inputs by adding a few plug-in modules. A *RAMM* 1024 charge storage memory (Standard Logic, Inc., Santa Ana, California) arranged for use as a 1024 x 8 bit data storage unit holds information until a paper tape is punched. The motorized paper tape punch (Model 2, Friden, Inc., San Leandro, California) can punch frames at 16.667 Hz.

The control circuitry to interface the three major components is primarily transistor-transistor logic (TTL) integrated circuits running on a 20 kHz system clock signal generated from a 2 MHz crystal oscillator (Figure 1). Gating circuitry and front panel rotary switches permit data sampling at rates from 0.0025 Hz to 20 kHz, i.e., once every 400 sec to 50 μsec. The DAS-16 unit digitizes ±10-V analog signals to 12-bit resolution. The 12-bit words are split into two groups of six bits each to permit storage in two 8-bit word locations in the memory and similarily on 8-bit paper tape (Figure 2). The paper tape bit arrangement uses one bit (No. 8) to indicate to the data analysis equipment the presence of data on the tape. The No. 7 bit distinguishes the most significant six bits from the least significant six bits. Bit Nos. 1-6 are the data bits themselves.

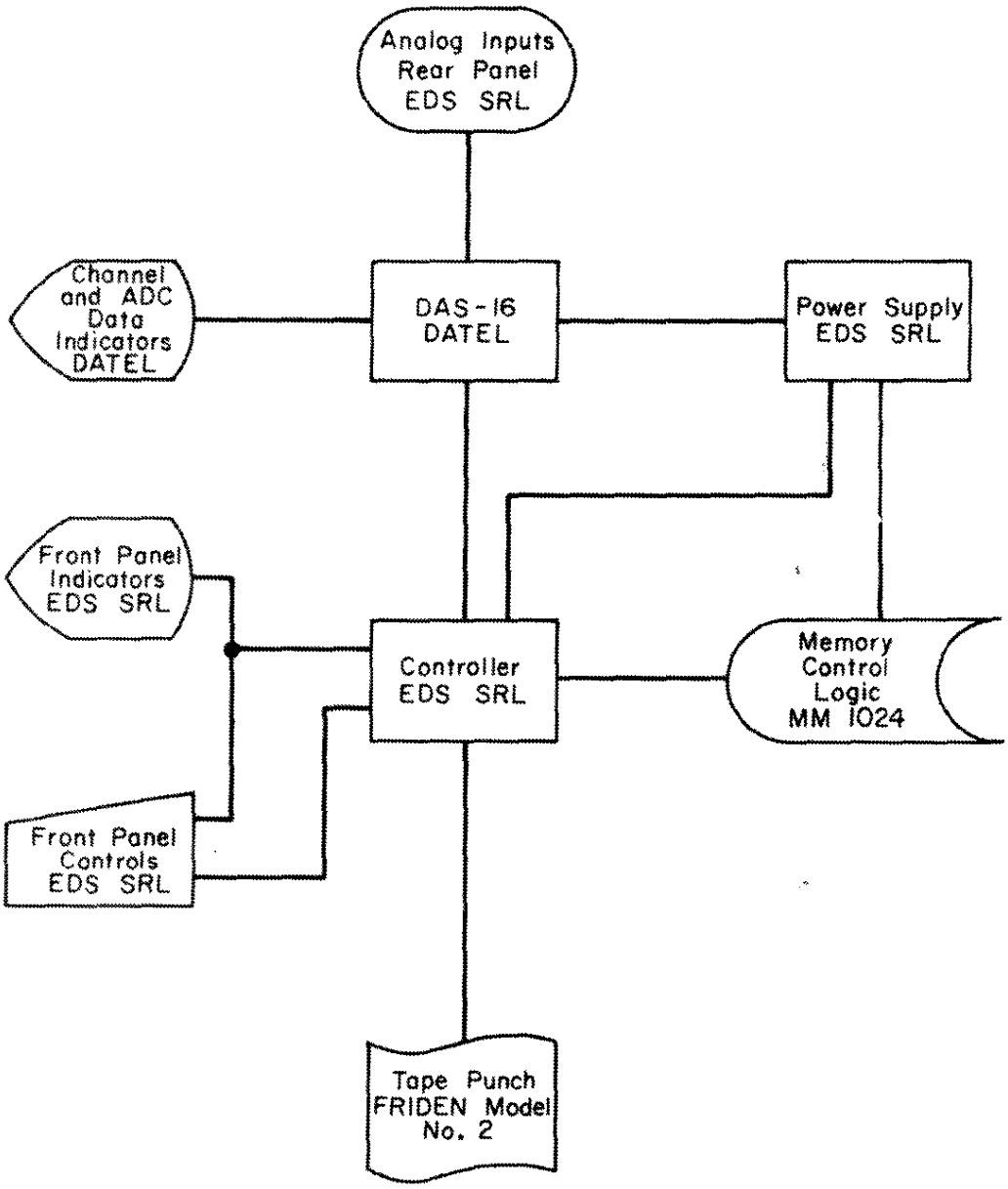

FIGURE 1. Logic Flow Chart

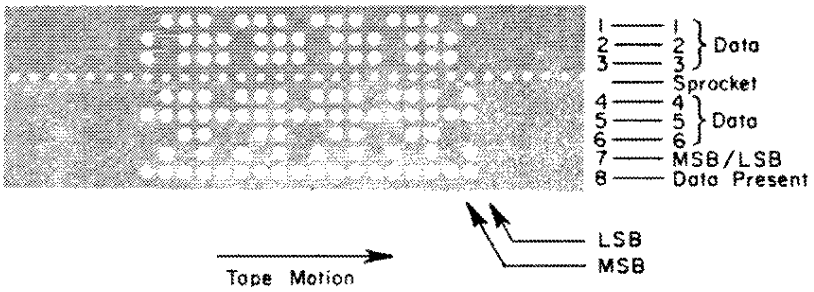

FIGURE 2. Specimen of 8-Bit Paper Tape

Existing teletype paper tape readers have data bit designations and sprocket holes exactly reversed from the *Friden* punch. Data tape may be simply turned face down and read into the teletype to facilitate data analysis.

Data are stored in the memory identically to the paper tape format. Depending on how many signals are sampled, data points range from a maximum of 512 per channel for one channel to 64 per channel when sampling all 8 inputs. The analog-to-digital converter (ADC) digitizes to ±1.0 bit out of 2048 with a signal resolution of 9.8 mV per bit.

FUNCTION OF CIRCUITS

Timing Circuit

The system clock, derived from a 2 MHz crystal oscillator, runs at 20 kHz. This rate was chosen because each memory system plane must be refreshed at least once every 2 msec. The internal arrangement of storage and refresh circuitry refreshes the 32 x 32 x 8 matrix of storage cells at one plane of 32 x 8 cells at a time. Therefore, refresh clock pulses theoretically must occur at least once every 62.5 µsec; in this system refresh pulses occur once every 50 µsec. The "memory refresh" cycle is required because the storage cells use interelement capacitance of the metal oxide semiconductor (MOS) and field effect transistor (FET) cell array to maintain the high or low state charge. The data storage charge decays with time, thus inferring a "dynamic" memory.

Data Acquisition Circuit

The "data-acquire" button (a magnetic field effect, solid state device) and the device-select flip-flop circuit enable the sample

rate clock count-down circuits and the DAS-16, and set the DAS-16 converter-to-memory buffer to divide the 12-bit data word into two 8-bit words for storage in the memory. The device-select flip-flop circuit also initiates the memory write controls and disables the punch output buffer.

The acquisition of data can be stopped at any time by depressing the "stop data acquire" button. This action latches in the last memory location used and disables the DAS-16 "strobe and device select."

Remote start-stop inputs on the front panel, a modification to photographed equipment (Figures 3 and 4), allow external commands to start and stop the "data-acquire" mode at times synchronized with outside events. Pulsed operation or level change operation from equipment to be monitored is possible (Figure 5).

Data Input Circuit

The DAS-16 module is fixed in the "sequential-sample" mode but may be changed by the front panel control to short cycle the input channels starting at Channel 0 and ending with any of the 16 available channels (Channels 0-7 operational). The front panel display of the DAS-16 indicates the channel number and the digitized value of the analog sample. The DAS-16 analog inputs (on the input panel at the rear of the rack) accept ±10-V inputs applied directly to the DAS-16 connectors. The rate at which the DAS-16 can sample data is any combination of the significant digits 2.5, 5, 10, or 20 and multipliers 10^{-3}, 10^{-2}, 10^{-1}, 10^{0}, 10^{1}, 10^{2}, or 10^{3} Hz. This provides the desired frequency of 3-μsec strobe pulses to the DAS-16.

Memory Circuit

The memory receives "initiate" and "write" commands at the conclusion of the DAS-16 analog-to-digital conversion cycle. Since the single 12-bit data word must be stored in two memory words, circuitry must provide for memory address incrementation and memory initiate and write commands from two sources. The DAS-16 begins the sequence, and then the last half of the data word is brought in by the memory. At the conclusion of this operation, the "memory address" flip-flop, the memory "initiate" and "write" flip-flops, and the "data word divider" flip-flop are returned to their "new data word" state to await information from the DAS-16.

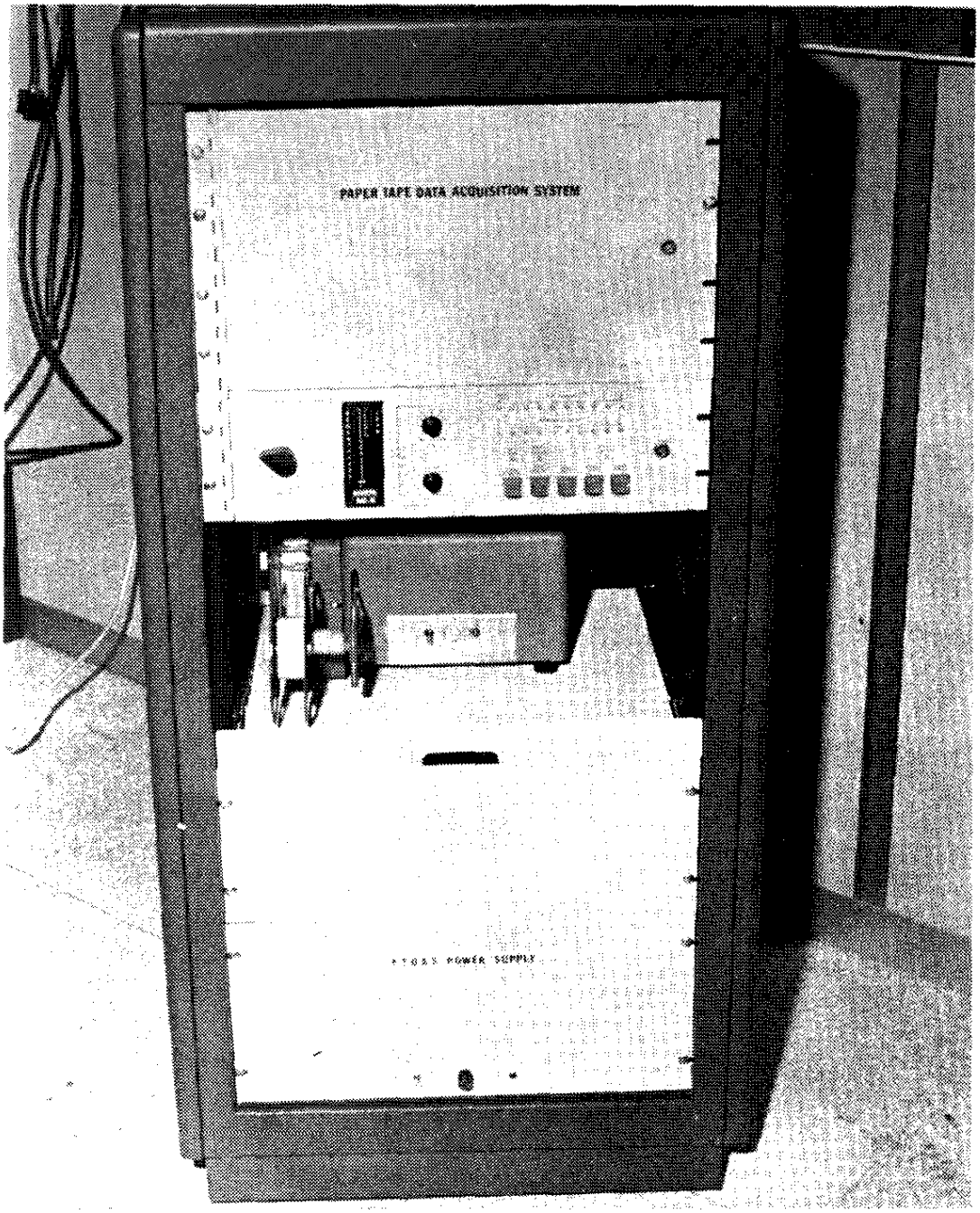

FIGURE 3. Logic Frame (Front View)

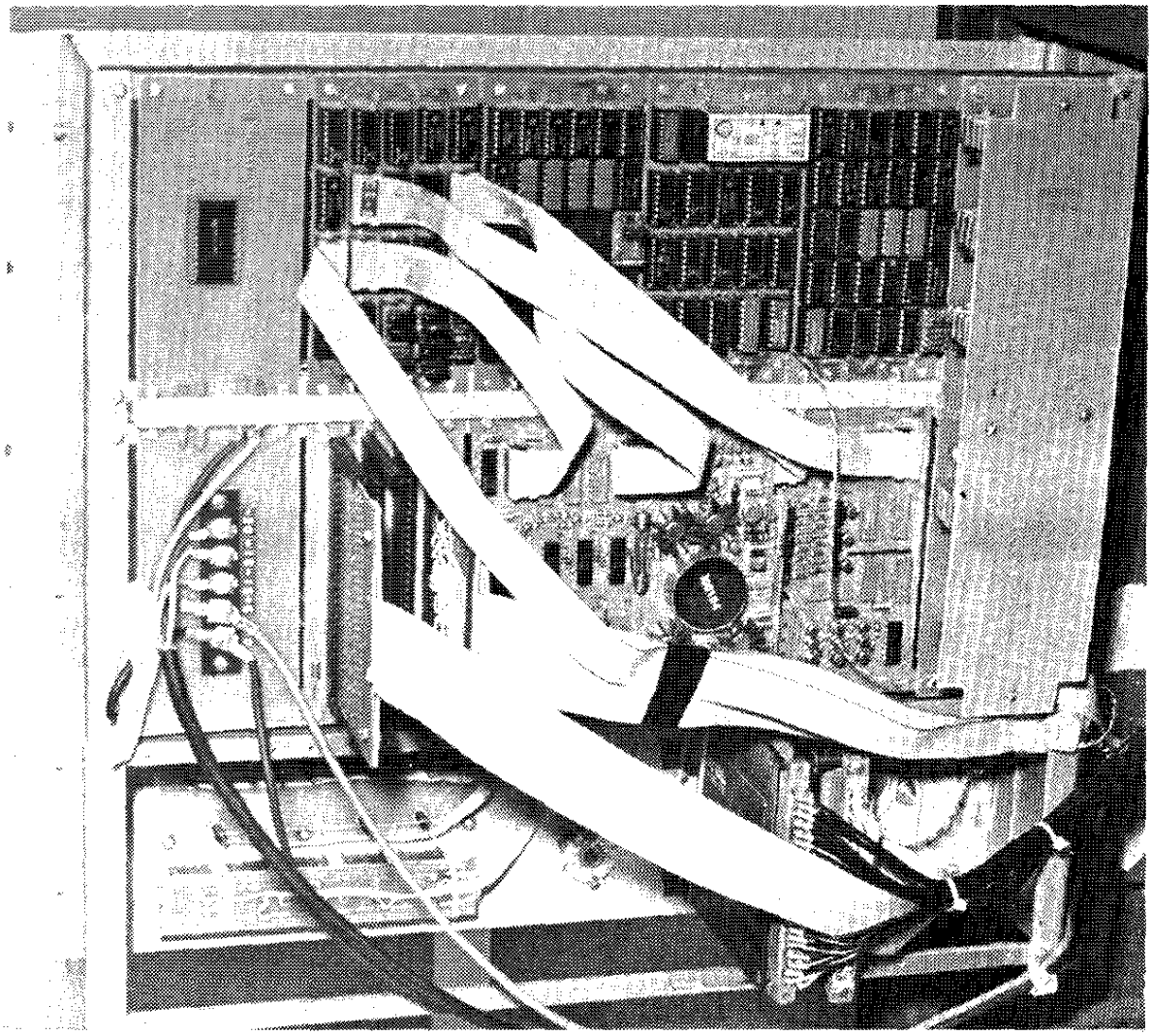

FIGURE 4. Logic Frame (Rear View)

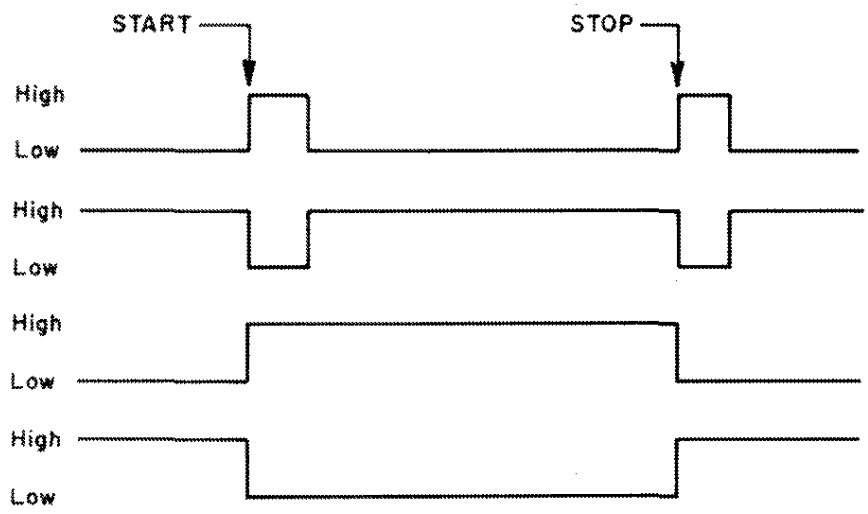

FIGURE 5. Start-Stop Input TTL Wave Forms

Provided in the equipment is a monitor to automatically end the data run when the memory is filled, thereby preventing eradication of previously gathered data. At this point, data will remain in the memory until new data are stored by the start of a new run or until power is lost to the instrument.

Paper Tape Circuit

Paper tape may be punched at the operator's convenience and may also be repunched should the paper tape punch fail, preventing data loss after the test is completed. The paper tape is punched after first preparing the equipment by resetting the punch. This initiates the last location flip-flop and the paper tape word flip-flop. By depressing the "tape feed" button, paper tape leader is generated containing only sprocket holes. After sufficient leader is obtained, the "tape feed" button should be released. When the "start punch" button is depressed, the punch will begin to cycle, reading from memory and punching tape until the information contained in the memory at the last location is on tape. When the punch stops, depressing the "tape feed" button will add trailer to the tape to complete the operation.

The *Friden* paper tape punch is interfaced to the memory through infrared optical couplers. The punch and clutch coils are powered by 135 VDC switched by high voltage power transistors. Diode spike suppressors are installed inside the punch across each coil. External line noise suppression is provided by a 500 W isolation transformer mounted at the lower rear of the rack.