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A DESK-TOP MICROCOMPUTER

J. S. BYRD

E. I. du Pont de Nemours & Co.
Savannah River Laboratory
Aiken, S. C. 29801

PREPARED FOR THE U. S. ATOMIC ENERGY COMMISSION UNDER CONTRACT AT(07-2)-1

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by

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Laboratory Operations and Services Division

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ABSTRACT

A low-cost desk-top microcomputer was designed and fabricated using an Intel Model 8008 central processor module. Programs can be sequentially loaded into a 2K x 8-bit random access memory with an octal data entry keyboard. Other key operations include single-point and sequential data readout, clear data entry, program interrupt, and program single cycle operation. Programs can be permanently stored in a 1K x 8-bit programmable read-only memory. All circuits were realized with plug-in dual in-line integrated circuit modules and wire-wrap connections.

This paper discusses applications of the microcomputer as a training aid and for process control. A control program that operates a process simulator chassis is also discussed. Several test programs are included in the appendices.

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I. INTRODUCTION

I.1 HISTORY OF THE MICROCOMPUTER

Recent advances in the state-of-the-art of microcircuit technology have made commercially available a large number of digital logic systems in the form of medium-scale-integration (MSI) and large-scale-integration (LSI) modules. These modules contain complex and large circuits combining the functions of many families of standard integrated circuit (IC) modules. The most significant development in this field has been the development and fabrication of the entire central processor (CP) of a computer on a single semiconductor chip, and is packaged in a single LSI IC module.[1] Several U. S. Manufacturers and one Japanese manufacturer have CP modules, in either the form of a single chip or a combination of several chips that contain all the processing power available in the early minicomputers.[2-6]

The first CP module, a four-bit parallel system, was introduced in 1971, and an eight-bit version was available in early 1972. These two products, Model 4004 and Model 8008 by Intel Corporation, Santa Clara, California, began the "computer on a chip" revolution, which now involves the entire electronics industry. The Model 8008 is being used in more applications than any other available module; within the past year (1972-1973) the unit price has dropped from over $200 to around $120.

I.2 THE MICROCOMPUTER'S IMPACT ON INDUSTRY

Since the emergence of the CP chip, several complete microcomputer systems have been developed using LSI modules.[7-11] They are being offered primarily as original equipment manufacturing (OEM) products to be built into user oriented and user developed systems. Software support is beginning to emerge on the scene, and microcomputer systems development products are available to reduce the costs of in-house systems development.[12,13] At least one company is marketing a complete 16-bit processor on a single printed circuit (PC) card.

Other MSI/LSI products are being developed that can be used with the CP modules in microcomputer systems.[15] Developments in improved semiconductor memory modules[16-18] will lower systems costs and improve performance. At present, semiconductor static memory modules are readily available in maximum bit capacities of 1024-bit random access memories (RAMs), 16,384-bit read-only memories (ROMs),

and 2048-bit programmable read-only memories (PROMs). Dynamic RAMs are available in sizes up to 4096 bits.

Microcomputers are not yet presenting a serious threat to the larger minicomputer systems due to their lack of software and their relatively slower processing speeds. A typical microprocessor executes an instruction in 10 to 60 microseconds. Faster modules using N-channel technology are being designed and should be available in 1974. Ten companies[19] are now deeply involved in the development of improved microcomputer modules and systems. Applications of future microcomputers should be limited only by the imagination of designers, programmers, and users.

I.3 THE PROBLEM

This research and development project was conducted to explore the potential use of presently available microprocessor modules in the areas of education and process control. A microcomputer system was fabricated, and its design, operation, and potential applications are discussed in the following sections.

A small, low-cost, general purpose computer is needed for use as a training aid for electronic engineers and technicians. In-house computer training is required to update engineers on computer hardware and software design techniques and to provide maintenance training for engineers and technicians. Textbook material on the subject needs supplementing with "hands on" experience with computers and digital logical circuits. The Desk-Top Microcomputer can provide this better than a larger computer system.

A low-cost microcomputer has unlimited uses in systems development and has direct applications to data formulating, data acquisition, and on-line process control. This project demonstrated the microcomputer's practicality and ability in these areas.

The author assumes that the reader of this report has a thorough understanding of digital logic and computer systems. A detailed description and the operating philosophy of the CP module, Model 8008, used for the microcomputer system are not included in this report. The Intel Model 8008 was selected for its proven reliability and availability, low-cost, and single 16-pin dual in-line package (DIP) module feature. The manufacturer's users manual[20] contains complete documentation necessary for a thorough understanding of operation of the CP module. Tables and diagrams pertinent to the circuit design in this report have been excerpted from that reference and appear in Appendix A.

II. DESIGN OF THE DESK-TOP MICROCOMPUTER

II.1 DESIGN OBJECTIVES

Design objectives for the Desk-Top Microcomputer were to minimize the cost and overall size with state-of-the-art components and modules and to realize a system where all signals would be easily accessible for circuit tracing.

With the training application in mind, the Desk-Top Microcomputer was designed with a wide variety of logic circuit techniques and modules. A straightforward logical approach was followed, resulting in circuit redundancy in a few instances, to allow easier troubleshooting and circuit tracing. For some logical functions, such as binary-to-octal decoding, standard transistor-transistor logic (TTL) IC modules were used in lieu of an MSI module to demonstrate the different types of circuits. Programs can be entered and data read out as octal and binary numbers to help the student acquire proficiency with those numbering systems (Appendix B).

II.2 ELECTRICAL AND MECHANICAL SPECIFICATIONS

The microcomputer (Figure 2-1) is housed in a sloping panel desk-top cabinet (10-in. x 14-in. base) with a hinged cover for easy access to all electrical circuits and components. The IC modules are plugged into a hinged socket assembly that can be supported in a vertical position to give access to the component side and the wire-wrapped circuit side, simultaneously (Figure 2-2). Light emitting diode (LED) assemblies are mounted in the hooded sloping panel section of the cabinet for easy viewing. The binary display lights are identified in groups of three so that displayed data can be quickly identified as octal numbers. All control switches and a 16-key keyboard data input are mounted on the top of the cabinet.

The design was realized with TTL (primarily 7400 series), LSI, and MSI logic modules. Details and circuitry of individual modules are in the manufacturer's design and applications handbooks[21-24] and in Appendix C. Point-to-point wire-wrapping was used for electrical connections. This method of wiring was selected as it is the only method in permanent IC circuits fabrication that allows easy circuit modifications. Prototype circuits for testing and analysis were not necessary, since circuit corrections could be easily made.

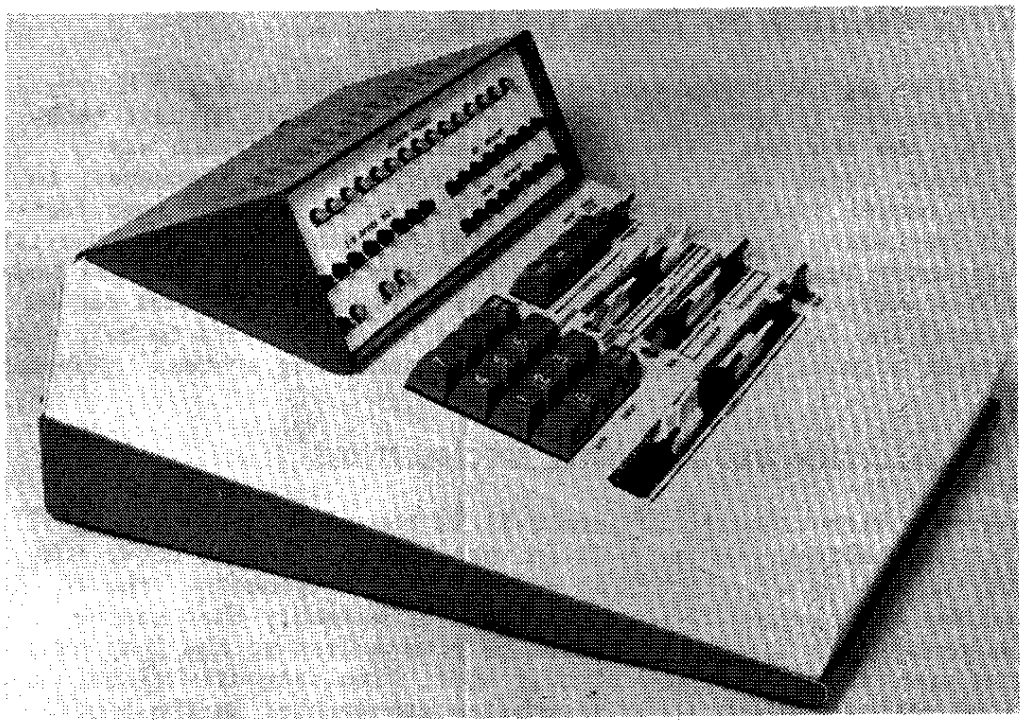
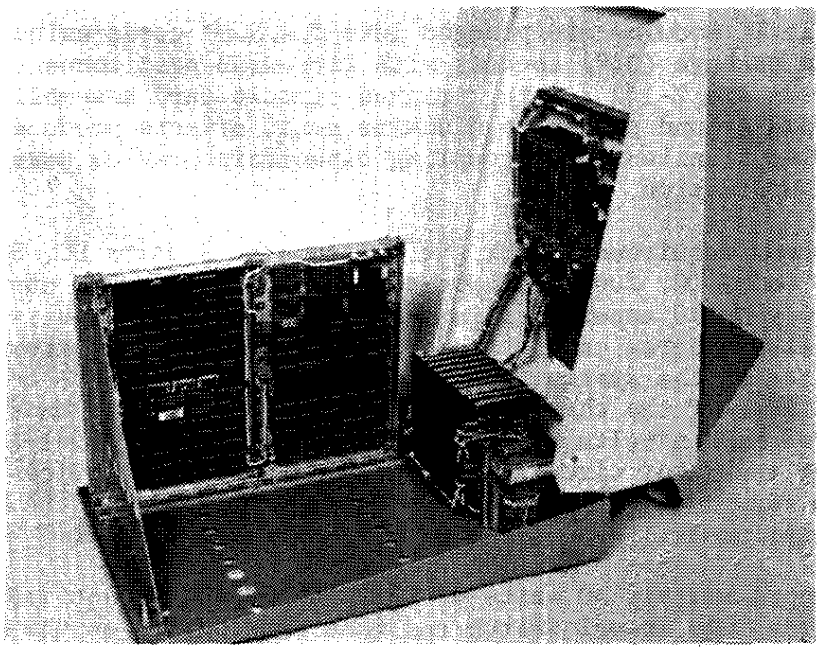
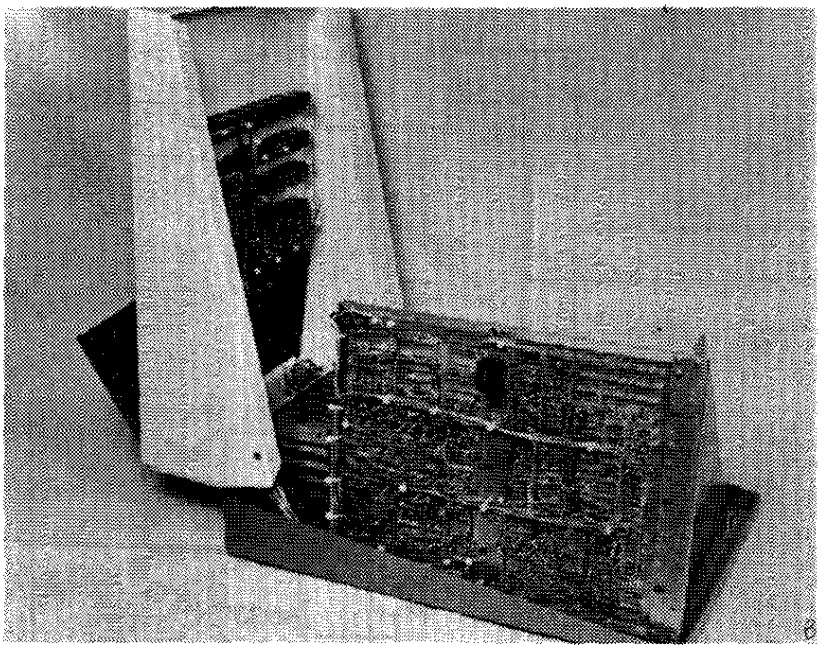


FIGURE 2-1. The Desk-Top Microcomputer



A. View Of Component Side Of Socket Assembly



B. View Of Wiring Side Of Socket Assembly

FIGURE 2-2. Microcomputer With Chassis Open

The IC modules are plugged into *C.A.S.H** cards using dual in-line package (DIP) sockets with wire-wrap post connections. The cards are 2-1/2 x 5-in. printed circuit card assemblies with power and ground planes to minimize noise effects produced by switching transients. Decoupling capacitors provide power supply noise suppression.

Power requirements for the system are +5 volts DC, 5.0 amperes, and -9 volts DC, 200 milliamperes. A compact +5 volt supply capable of supplying 10 amperes is installed in the microcomputer. The extra five amperes can be used to furnish power for external devices connected to the system through the input/output (I/O) connector on the rear of the chassis. Negative voltage requirements are supplied with a voltage doubler and an IC module, Model LM304, voltage regulator circuit (Figure 2-3). Only two devices in the system required -9 V power: the Model 1702 PROM and the MK 5009 interrupt clock.

Approximately 30 watts of 115V AC power are required for operation. An on-off switch and fuse are located on the rear panel of the cabinet to keep line noise pickup in the control signals at a minimum.

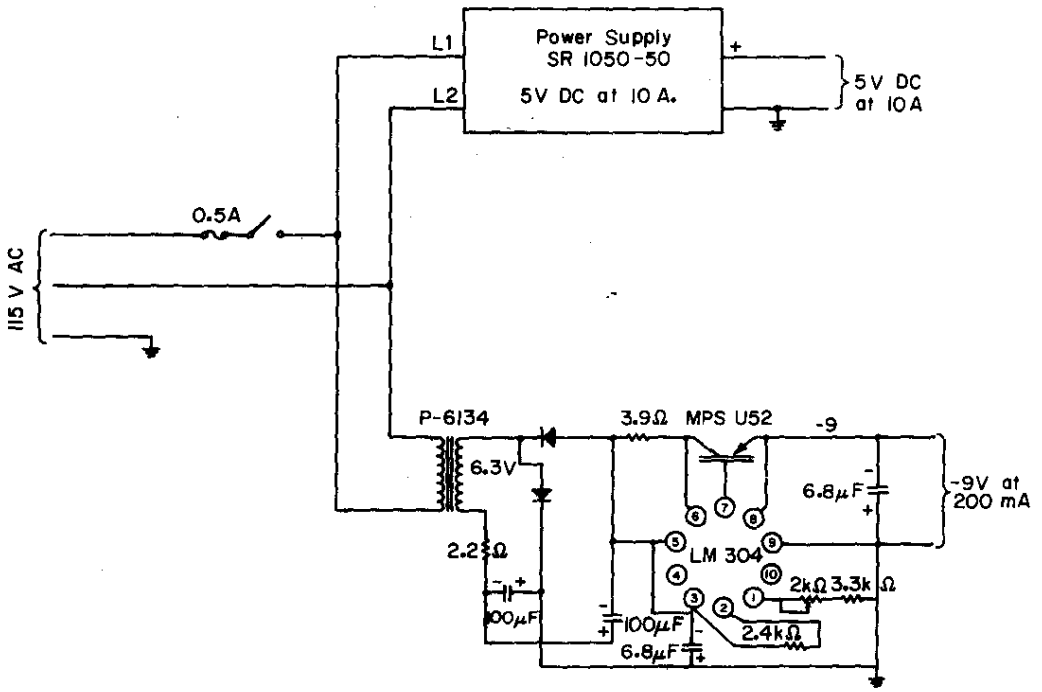


FIGURE 2-3. Power Supplies Schematic

* Registered trademark of Standard Logic, Incorporated, Santa Ana, California.

II.3 SYSTEM ORGANIZATION

The basic hardware of the Desk-Top Microcomputer is the same as that of a typical full-scale computer system. The major components of the circuit (Figure 2-4) are the central processor and timing logic, memory and control logic, data input keyboard circuitry, and the I/O logic. The next few sections discuss in detail the logic circuits.

Each logic function, gate, flip-flop, etc., shown on the logic diagrams is numbered (for example, A1-2, D2-3) to give the location of the respective plug-in DIP module in a socket array (Figure 2-5). Pin numbers of the inputs and outputs are on the diagrams so that each signal can easily be identified when troubleshooting. The types of modules are specified on Figure 2-5.

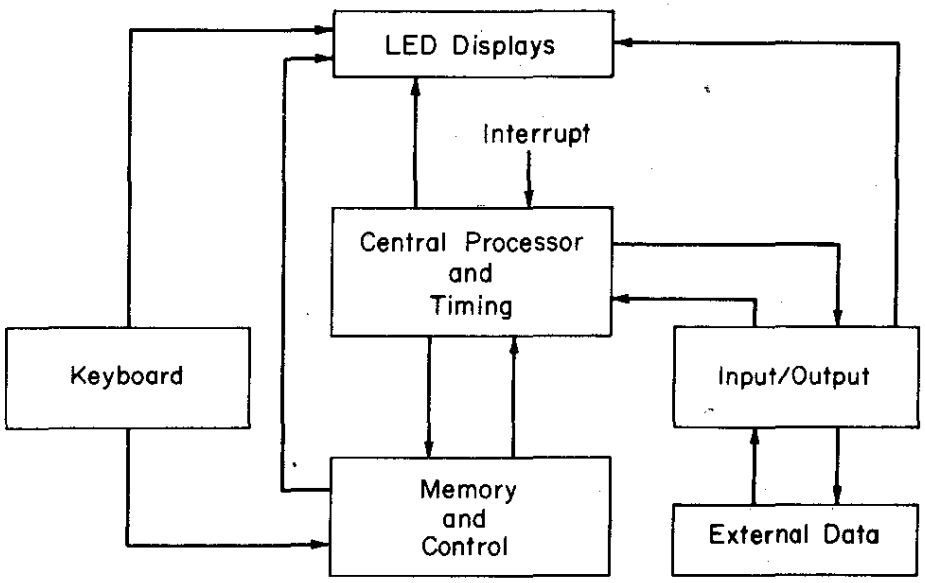
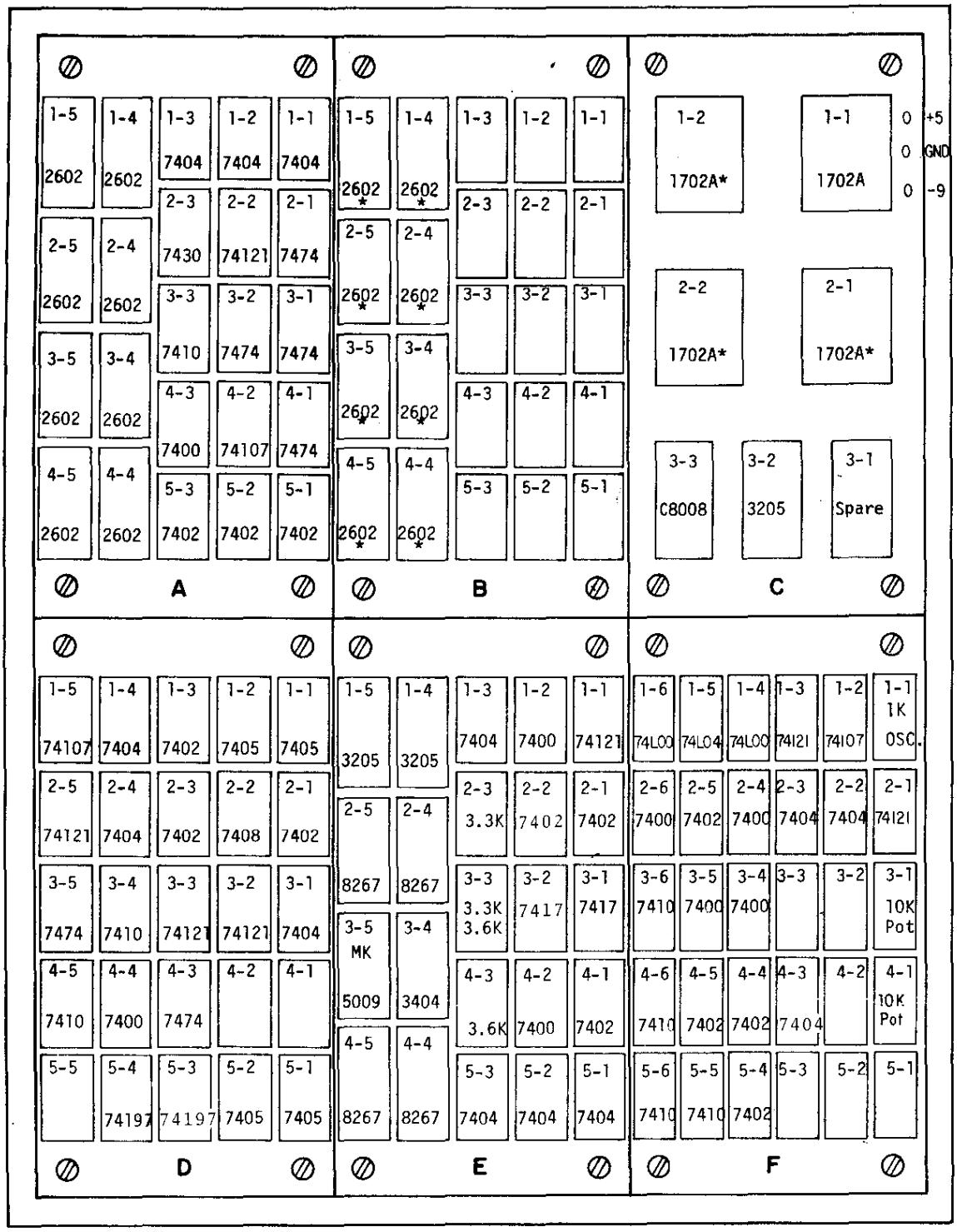


FIGURE 2-4. Simplified Block Diagram Of Microcomputer



*Wired But Not Installed In Prototype

Viewed From Wiring Side

FIGURE 2-5. Integrated Circuit Module Layout

II.4 CENTRAL PROCESSOR AND TIMING

The CP user's manual[20] supplements the remaining material in this section. The reader will find it most useful to refer frequently to the manual during discussions of the CP and associated circuits.

A one-megahertz (MHz) crystal oscillator module is divided by two with a flip-flop (F1-2) to provide the basic 500-kilohertz (kHz) timing for the Model 8008 CP module (Figure 2-6). Two single-shot multivibrators (F1-3 and F2-1) generate the two-phase clock signals, $\phi 1$ and $\phi 2$. Timing outputs from the CP are three state signals, S_0, S_1, S_2, and SYNC. These signals, along with the phase clock, are decoded and gated to provide all timing operations for the microcomputer (Figure 2-7). Output signals from an octal decoder module (Model 3205, C3-2) identify the eight states of the CP instruction cycle.

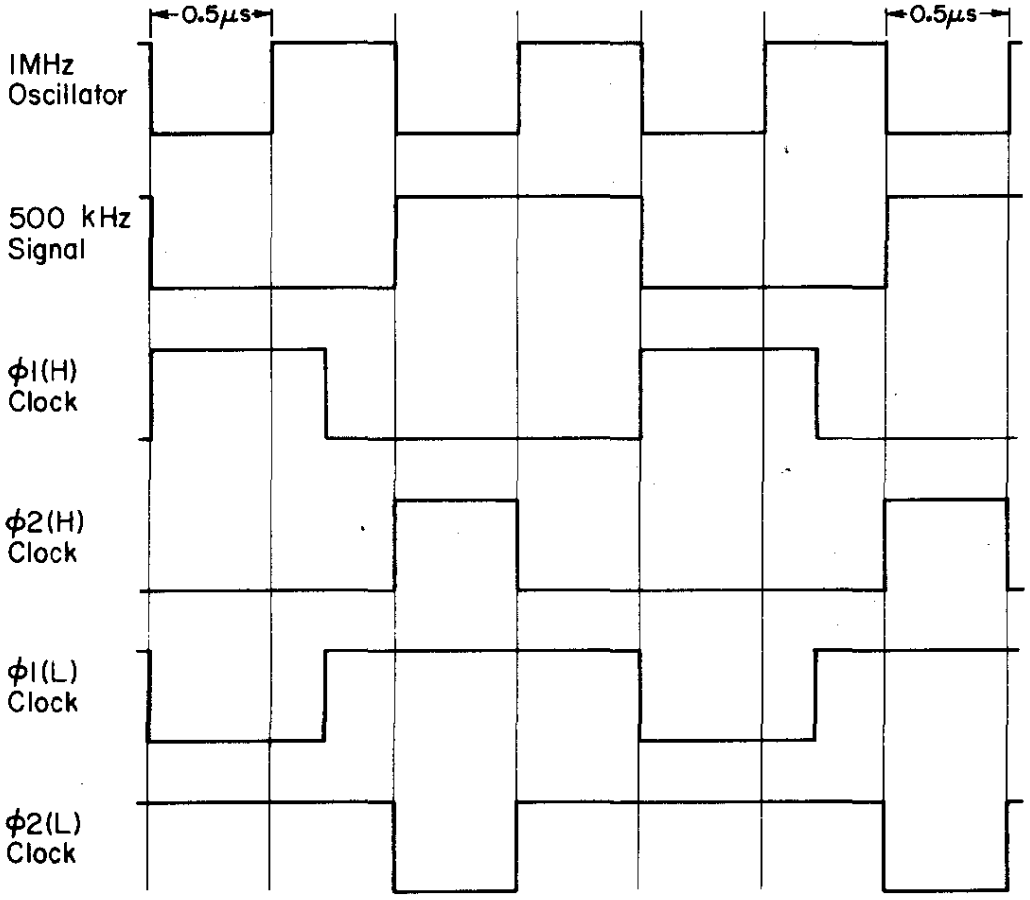


FIGURE 2-6. Clock Signals Timing Diagram

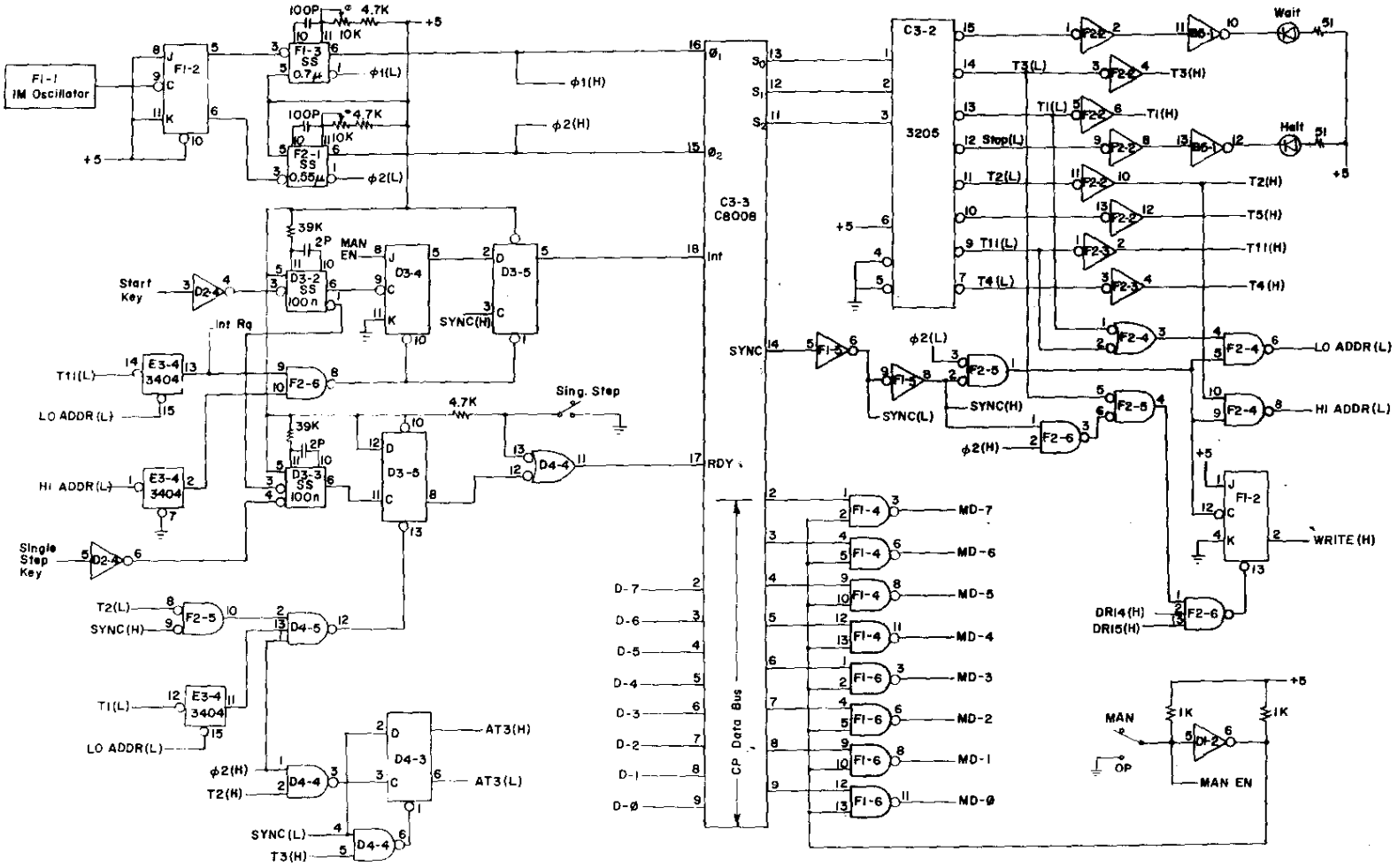


FIGURE 2-7. Central Processor Logic Diagram

A timing diagram (Figure 2-8) shows typical signals during the first memory cycle of an instruction. CP states Wait and Stopped are constant when the CP is idling in one of those states. States T1I is substituted for the normal T1 state during the first memory cycle if a program interrupt (INT) has initiated the cycle. During the memory address fetch portion of an instruction, logic signals LO ADDR(L)* and HI ADDR(L) gate the least significant byte and the most significant byte, respectively, from the CP address register on the CP data bus at states T1 and T2.

$$\text{LO ADDR(L)} = [\text{T1(L)} + \text{T1I(L)}] \cdot [\phi 2(\text{L}) \cdot \text{SYNC(H)}] \qquad (2.1)$$

$$\text{HI ADDR(L)} = \text{T2(H)} \cdot [\phi 2(\text{L}) \cdot \text{SYNC(H)}] \qquad (2.2)$$

For instructions requiring an eight-bit byte of data to be inputed to the CP during T3 state, an "anticipated T3" state signal, AT3(H), is generated by a type D flip-flop (D4-3). This signal goes true

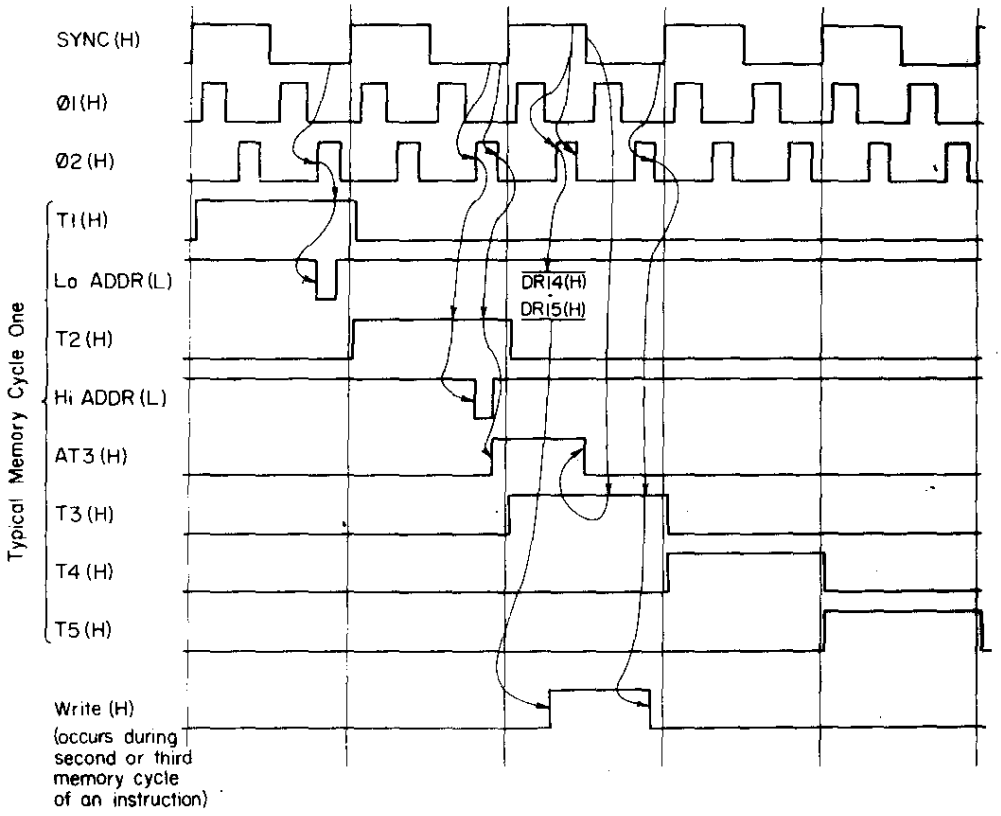


FIGURE 2-8. Instruction Cycle Timing Diagram

* An "H" and "L" in parentheses at the end of a logic signal name indicates a high-true or a low-true signal.

during the T2 state to ensure that data are on the bus before the CP is ready to read the data during the first half of state T3.

When data are written into memory during the second or third memory cycle of an instruction, WRITE(H) is generated in state T3 by a J-K flip-flop (F1-2). The leading edge of WRITE(H) is synchronized with $\phi 2(H) \cdot \overline{SYNC(H)}$ during the first half of state T3. Its trailing edge is synchronized with the trailing edge of $\phi 2(L)$ near the end of state T3. DR1(H) and DR15(H) must be true (Table 2-1), indicating a memory write operation, before WRITE(H) is initiated.

TABLE 2-1. ADDRESS CONTROL BITS

Data Register		
DR 15	DR 14	Instruction Function
0	0	Address is for a memory read operation (instruction fetch cycle)
1	0	Address is for a memory read data operation (additional bytes instruction or data)
0	1	Data are for a command I/O operation
1	1	Address is for memory write operation

Initial startup of a program is accomplished with the program interrupt circuitry. When the power is turned on, the CP clears its internal registers and stops in the Halt state. If the interrupt line (INT) is pulsed with a high-true signal, the CP enters the TI1 state then proceeds through the complete program cycle, T2, T3, etc. During that program cycle a one-byte instruction is read in from the Interrupt/Instruction switches and executed. Normally, a restart instruction (RST) is set in the switches. RST is a one-byte instruction that calls a subroutine beginning at addresses 000, 010, 020, 030, 040, 050, 060, or 070 in the PROM.* These locations normally contain a jump instruction (JMP) to the main program located elsewhere in the PROM or RAM. For example, if instruction 065 was set on the Interrupt/Instruction switches,

* All instructions and addresses in this report are given as octal numbers.

TABLE 2-2. TYPICAL STARTUP ROUTINE

PROM Address	Octal Instruction	Explanation
060	104	Unconditionally jump
061	000	to location 4000
062	010	in memory.
↓		
4000	300	Program address
4001	300	counter has advanced
4002	300	to 4000; CP continues
4003	300	the program, sequentially.
•	•	
•	•	
•	•	
5000	377	Program Halts at memory location 5000

depressing the START key would initiate a startup program beginning at address 060. A very simple program may jump to begin a more complex program at address 4000 (Table 2-2).

The leading edge of INT is synchronized with SYNCH(H). The trailing edge of INT is synchronized with ϕ2(H) near the end of T2 state (Figure 2-9). If the machine is operating in a normal RUN mode (Single Cycle switch in down position), the program continues to run until a HLT instruction is received. With Single Cycle mode selected, ready signal (RDY) to the CP is initially inactive, or low. Depression of START key will activate RDY long enough for the initial one-byte instruction to be executed and will return to its inactive state at the end of state T2 of the following instruction. The CP will then stop in WAIT state. Each time the SINGLE STEP key is depressed, the CP will execute one memory cycle and return to the WAIT state.

An interrupt clock may be turned on to initiate a program interrupt at approximately one-fourth-second intervals. The frequency can be changed by rearranging jumpers (pins 11-14, E3-5) of the MK5009 module (Appendix C, Section C.3.).

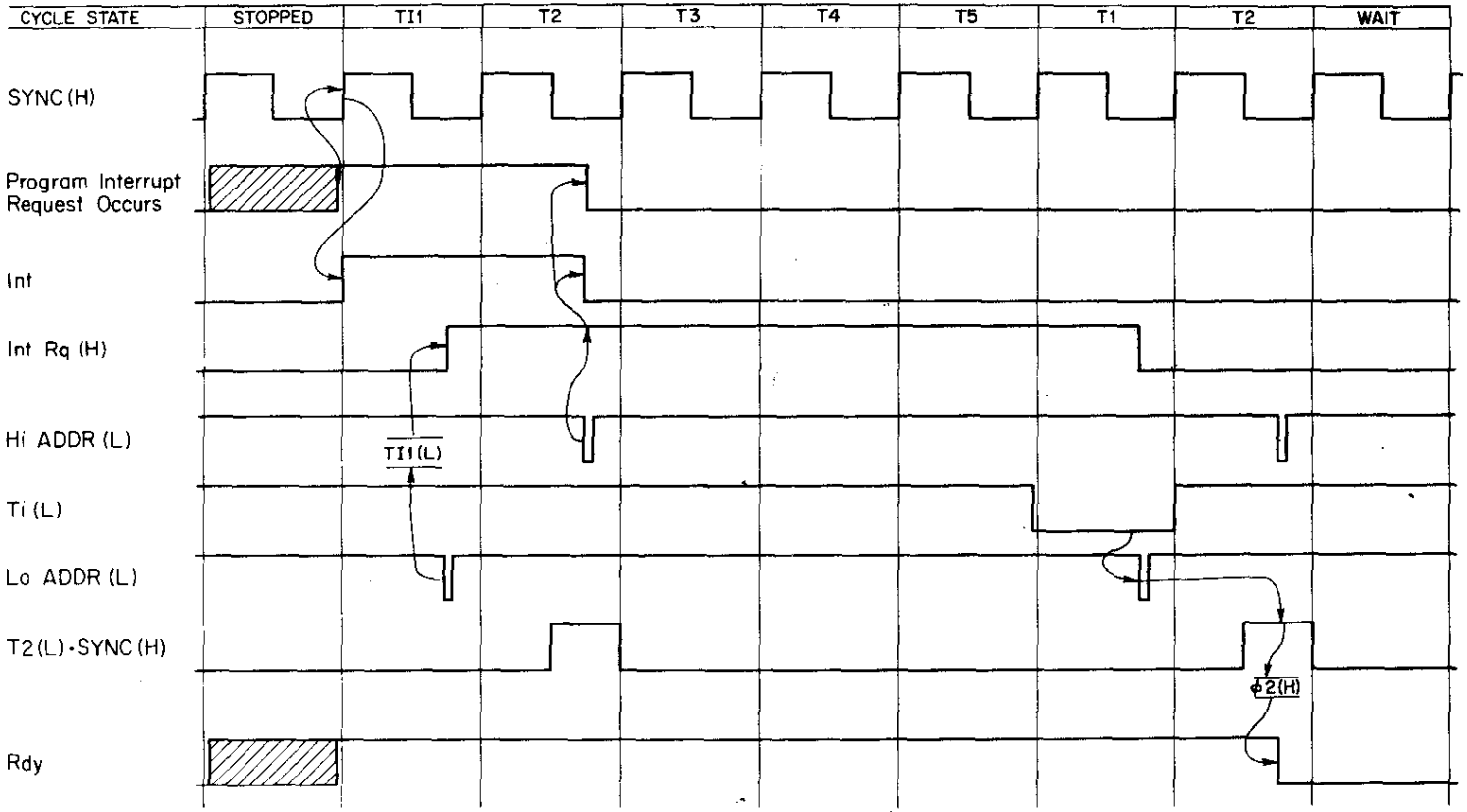


FIGURE 2-9. Interrupt/Ready Timing Diagram

II.5 MEMORY AND MEMORY CONTROL

Sixteen bits (two bytes) of data from the gated CP bus outputs, MD0-MD7, are clocked into MSI register/counter modules, Model 74197 (Figure 2-10, Modules B1-1, B2-1, B3-1, B4-1), with LO ADDR(L) and HI ADDR(L). The most significant two bits are for control purposes; the remaining fourteen are for memory address or data. Two octal decoders (E1-4 and E1-5) provide eight memory select lines for PROM selection and four lines for RAM modules. When operating in the Manual mode, MAN EN(H) disables the CP bus to the No. 74197 module inputs and enables the Address switches on the control console. For this condition, LOAD DR(H) latches the Address switch to the register/counter. In Manual/Increment mode, INC DR(L) increments the counters each time a new memory data byte is deposited or examined.

The PROM modules (Figure 2-11) are Model 1702 metal oxide semiconductor (MOS) P-channel devices,[21] each containing 256 eight-bit words complete with decoding logic. The memory chip may be erased by exposure to ultraviolet light through the quartz lid and reprogrammed with an external programmer. Four PROMs may be plugged directly into the circuit (sockets C1-1, C1-2, C2-1, C2-2). Select lines (CS1-8) are available for a total of eight PROM modules.

The RAM modules are Model 2602 MOS N-channel devices,[24] each containing a 1024 x 1-bit memory array with decoding logic. These devices, static RAM modules, were selected so that refreshing logic, required for less expensive dynamic RAMs, was not necessary. Also, the 2602 modules require only a 5-volt power supply. Read-time and write-time are approximately one microsecond each. Sixteen RAM modules may be plugged in for a total RAM capacity of 2000 x 8 bits. Each 1K RAM module is activated by one of four select lines, CS9-12.

As both N-channel and P-channel devices are involved, the outputs of the PROM and RAM modules cannot be directly OR-tied or bussed together. These modules are connected through NOR gates.

Address inputs for the memory are DR0(H)-DR9(H), outputs from the register/counter latch modules (Figure 2-10). Data inputs are MD0-MD7 from the CP bus and DI0-DI7 from the data input keyboard. Write command signals for the RAM are WRITE(H) from the CP control circuitry and LOAD RAM from the data keyboard logic. When not enabled with a CS select line, the PROM and RAM modules are in a high impedance output state requiring pull-down resistors at the outputs to hold the gate inputs low (E2-1, E2-2).

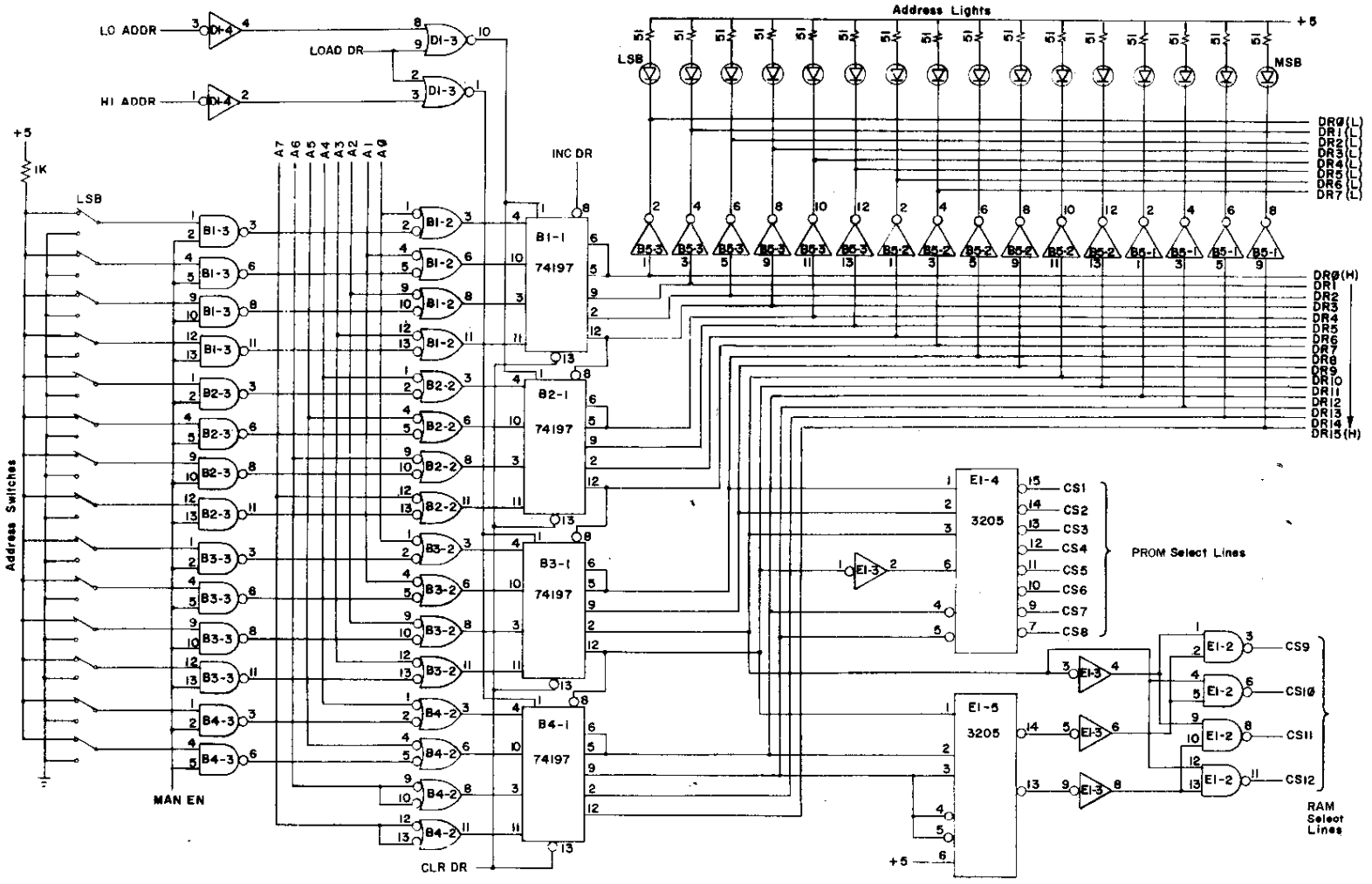


FIGURE 2-10. Memory Control Logic Diagram

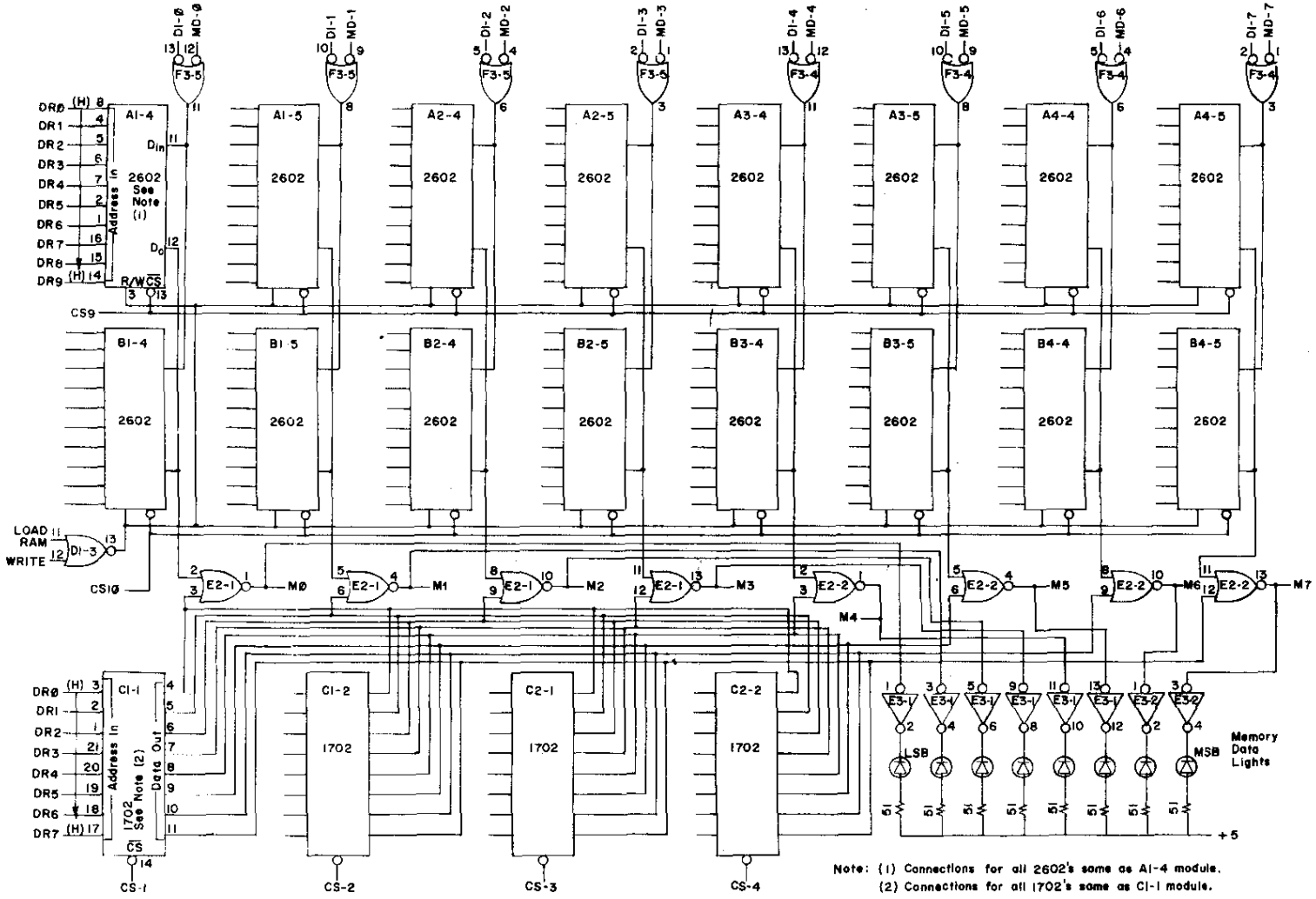


FIGURE 2-11. Memory Modules Logic Diagram

II.6 INPUT/OUTPUT LOGIC

The I/O instructions, INP and OUT, are two-cycle instructions. During the second memory cycle, the instruction is transferred from the CP internal register "b" to the data bus at T2 state; the memory register/counter then contains the instruction. By decoding DR9(H)-DR13(H), the circuitry determines whether the instruction in progress is input or output and decides which one of the eight I/O conditions to activate (Table 2-3). Inverters and gates, TTL modules, make up a binary-to-octal decoder (Figure 2-12) to decode DR9(H)-DR11(H) for eight output pulses, OUT0(L)-OUT7(L). These pulses can be used to load latches with data from the CP accumulator, DR0(H)-DR7(H), or can be used alone as output control pulses. One output pulse, OUT1(L), is used to latch data into an eight-bit register (D5-4, D5-3); the outputs are displayed on the control console. OUT7(L) is connected to clear the DATA-1 register. The I/O pulses occur at T3 state in the CP cycle. Only four input control pulses are operative. INP0 and INP1 control inputs to a multiplexer (Model 8267, E4-4, E4-5).[24] The multiplexer control signals, S2-0(L) and S2-1(L), gate in data through the I/O connector (pins 19-26) and the console DATA-1 switches, respectively, to the CP data bus. The following equations for OUT7(L) and IN0(L) show the timing relationships:

$$\text{OUT7(L)} = [\text{AT3(H)} \cdot \text{DR14(H)} \cdot \text{DR15(L)}] \cdot [\text{DR12(H)} + \text{DR13(H)}] \cdot [\text{DR9(H)} \cdot \text{DR10(H)} \cdot \text{DR11(H)}] \quad (2.3)$$

$$\text{IN0(L)} = [\text{AT3(H)} \cdot \text{DR14(H)} \cdot \text{DR15(L)}] \, [\overline{\text{DR12(H)}} \cdot \overline{\text{DR13(H)}}] \cdot [\overline{\text{DR9(H)}} \cdot \overline{\text{DR10(H)}} \cdot \overline{\text{DR11(H)}}] \quad (2.4)$$

TABLE 2-3. INPUT/OUTPUT INSTRUCTIONS

Data Register Bits							Decoded Conditions
DR15	DR14	DR13	DR12	DR11	DR10	DR9	
0	1	X	X	X	X	X	I/O instruction in progress.
0	1	0	0	X	X	X	Input instruction in progress.
0	1	1	0	X	X	X	Output instruction in
0	1	0	1	X	X	X	progress.
0	1	X	X	0	0	0	I/O Device 0
0	1	X	X	0	0	1	I/O Device 1
0	1	X	X	0	1	0	I/O Device 2
0	1	X	X	0	1	1	I/O Device 3
0	1	X	X	1	0	0	I/O Device 4
0	1	X	X	1	0	1	I/O Device 5
0	1	X	X	1	1	0	I/O Device 6
0	1	X	X	1	1	1	I/O Device 7

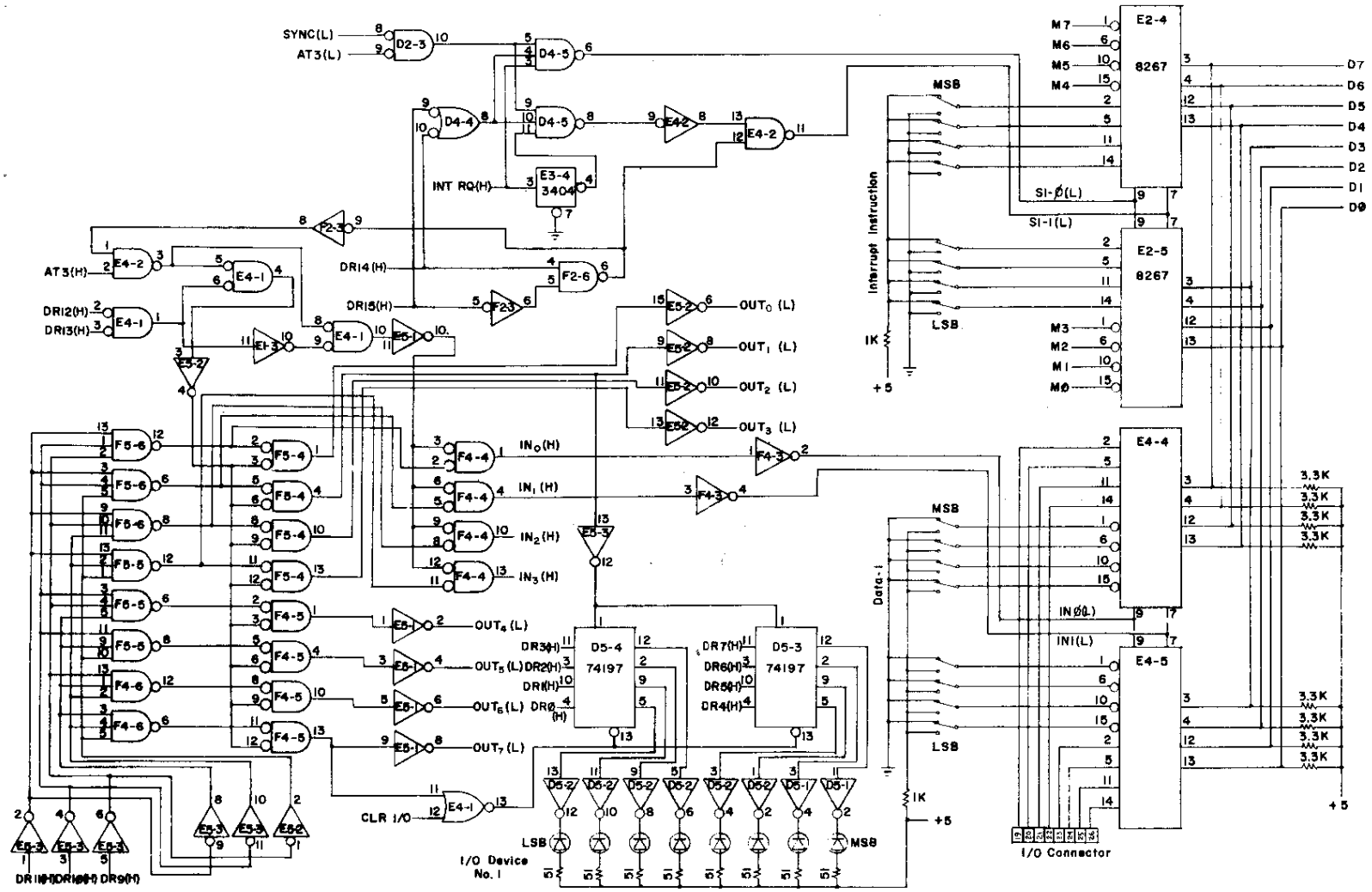


FIGURE 2-12. Input/Output Logic Diagram

A second multiplexer on the CP data bus (E2-4, E2-5) controls data from memory, M0-M7, and the Interrupt/Instruction Switches. Multiplexer control signal, S1-1(L), is active for memory data; S1-0(L), for an interrupt. The following equations describe their logic:

$$S1\text{-}0(L) = INT\ RQ(H) \cdot [AT3(L) \cdot SYNC(L)] \cdot [\overline{DR14(H)} + \overline{DR15(H)}] \quad (2.5)$$

$$S1\text{-}1(L) = INT\ RQ(L) \cdot [AT3(L) \cdot SYNC(L)] \cdot [\overline{DR14(H)} + \overline{DR15(H)}] \cdot [\overline{DR14(H)} + DR15(H)] \quad (2.6)$$

II.7 DATA KEYBOARD

The data keyboard provides a unique method to load octal program instructions into the RAM (Figure 2-13). The keyboard is a matrix of 16 Hall-effect pushbutton switches; the outputs are a "bounceless" high-true logic level when activated. Only 10 keys are wired for circuit functions. A sixteen-to-four line encoder module (Appendix C, Section C.2) converts the active key signal to a binary-coded-decimal (BCD) code. The depression of three consecutive octal keys loads an eight-bit register (A3-2, A3-1, A2-1, A4-1), generates LOAD DR to load the memory address register from the console switches, generates LOAD RAM to write the instruction into memory, and also increments the memory register with INC DR when operating in Increment mode. The memory register is cleared with CLR DR when the first instruction of a sequence is entered. A Mod-3 counter (A4-2) steers the first entered digit to the two most-significant bits in the data register (A3-2); the second digit, to the next three bits; and the third digit, to the three least significant bits. When the third number is depressed, LOAD DR is activated (D2-1); when released, LOAD RAM is generated from a single-shot multivibrator (E1-1).

A READ OUT key clears the memory address register, CLR DR, and loads the register with the console switch address, LOAD DR. In the Increment mode, the next READ OUT key depression increments the Address register with INC DR and reads out the next memory location. Memory data and addresses are displayed on console indicators. The Single Entry mode inhibits INC DR (D2-2).

A CLEAR ENTRY key clears the data register and Mod-3 counter. A RESET switch clears data register, I/O register, Mod-3 counter, and the memory address register. Outputs from the data register, DI-0 - DI-7, are OR-ed with CP bus data at the inputs of the memory modules.

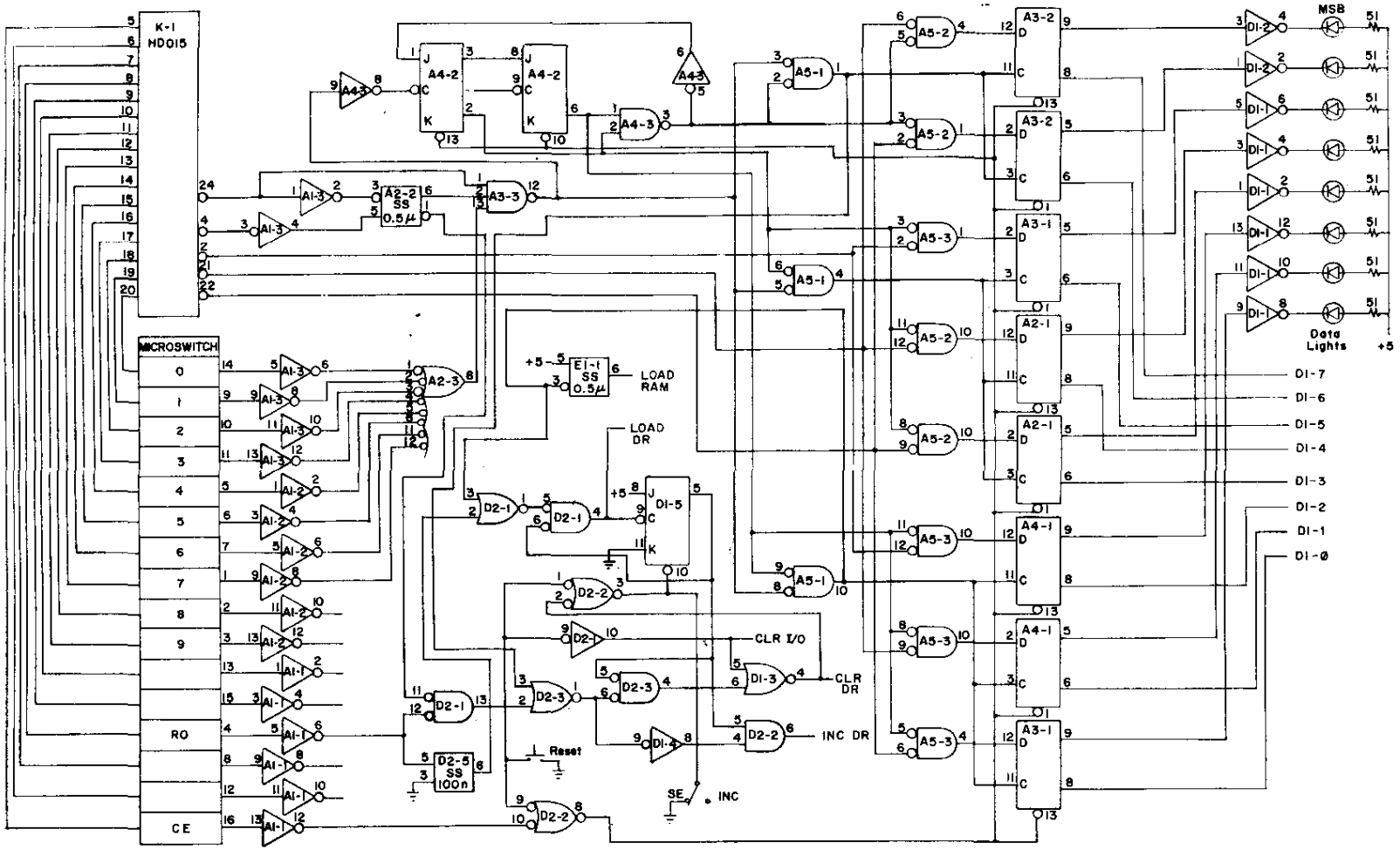


FIGURE 2-13. Keyboard Logic Diagram

II.8 PROCESS SIMULATOR

A separate chassis was designed and fabricated to demonstrate typical I/O capabilities of the microcomputer. This unit contains hardware to simulate a typical plant process. The microcomputer and the process simulator (Figure 2-14) are connected with a cable from the I/O connector on the microcomputer.

Two eight-bit latches (X10-X12) and two output control pulses [OUT2(L) and OUT3(L)] store data from the microcomputer when the instructions (OUT2 and OUT3) are executed (Figure 2-15). Outputs from the latches are connected to digital-to-analog converters (DACs) and LED display lights. One DAC (X4) is connected to a microammeter. Analog outputs (0-1V DC) are connected to BNC connectors on the rear of the simulator chassis.

Two flip-flops (X9) provide controls for high and low level alarm lights and a buzzer. To turn on the high alarm condition the microcomputer's accumulator must be loaded with a number that has bit-0 (LSB) true and bit-1 false just prior to the execution of OUT4 instruction. To set the low alarm, the accumulator must contain bit-0 false and bit-1 true prior to execution of OUT4.

An analog-to-digital converter (ADC) derives its 0-10V input from a ten-turn potentiometer in a voltage division network. The eight-bit output from the ADC connects to an input data port in the microcomputer. The output instruction, OUT0, resets the ADC with the leading edge of pulse OUT0(L) and starts the next con-

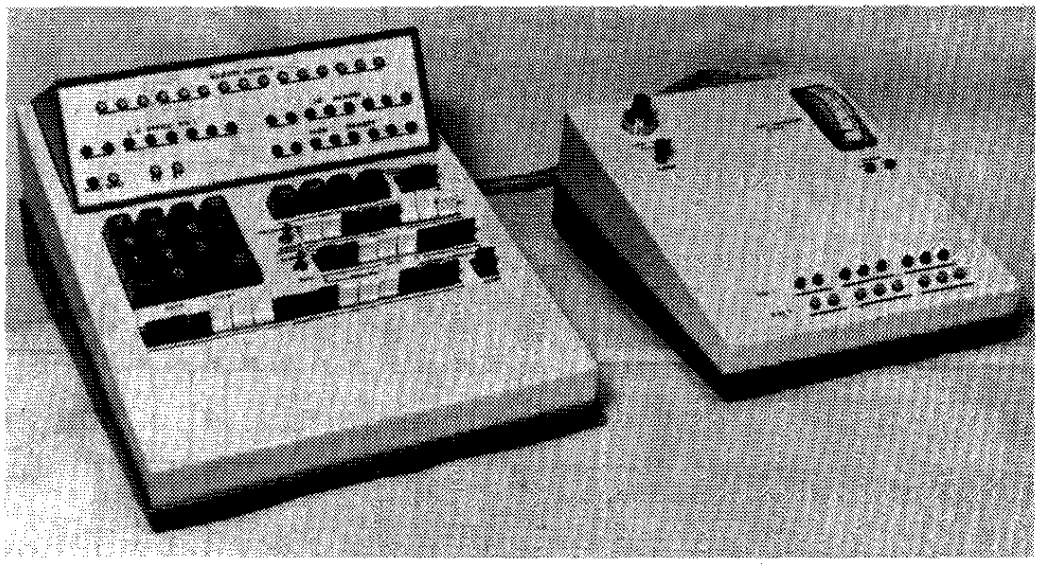


FIGURE 2-14. Microcomputer With Process Simulator

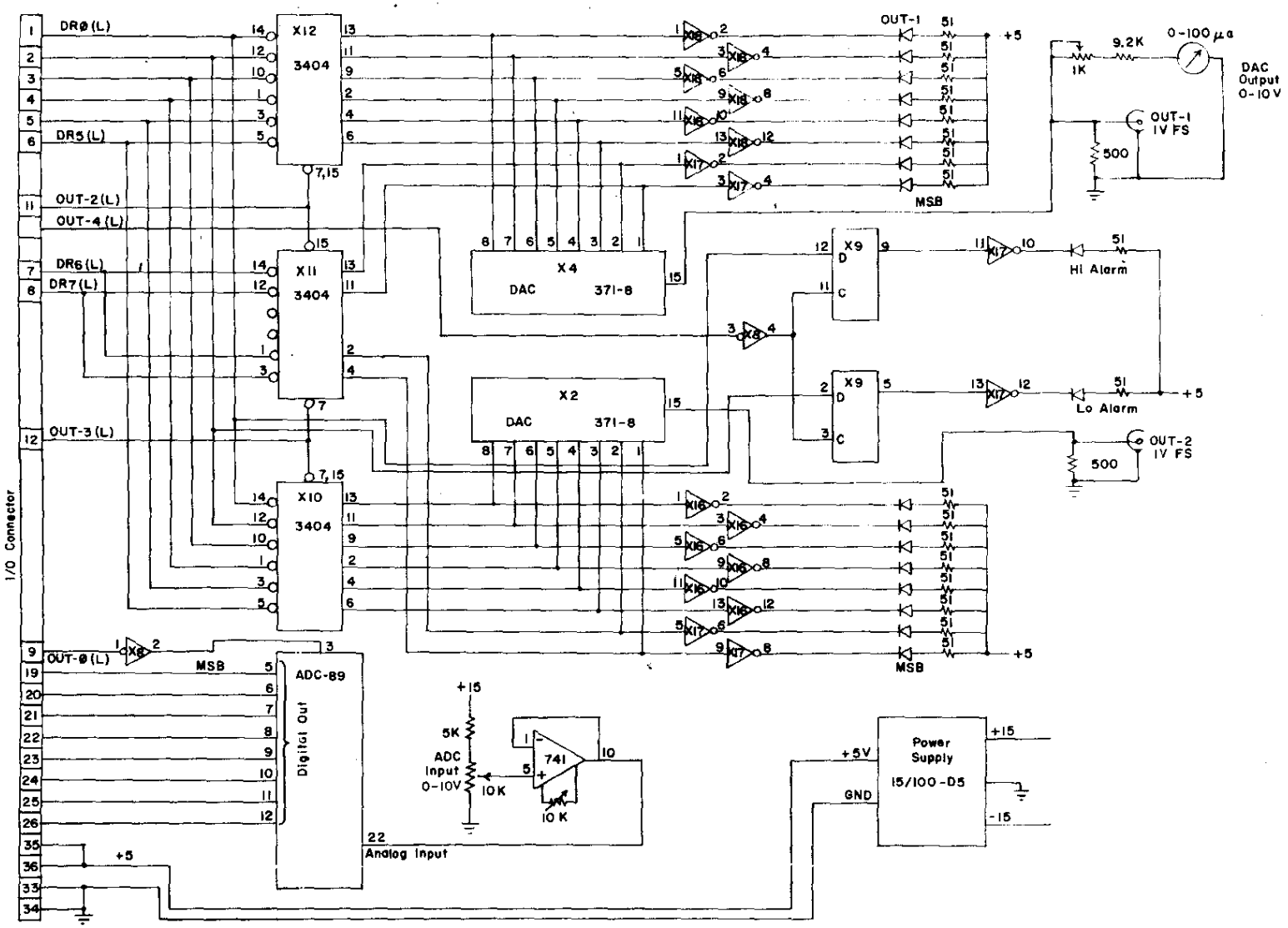


FIGURE 2-15. Process Simulator Logic Diagram

version with its trailing edge. Approximately 200 microseconds are required for an eight-bit conversion because the program must allow for that delay between OUT0 instructions. The ADC holds the digital data from a conversion in its internal buffer register until a reset pulse is received.

The +5V power for chassis is supplied from the microcomputer power supply. A DC-DC power converter, Model 15/100-D5, supplies ±15V to the analog modules.

III. OPERATION OF THE DESK-TOP MICROCOMPUTER

III.1 DESCRIPTION OF INDICATORS AND CONTROLS

III.1.1 Memory Address indicators

The Memory Address Indicators (Figure 3-1) are a group of fifteen LED indicators that display the fourteen least significant bits from the register/counter modules connected to the CP data bus. The most-significant bit of the display is inoperative and is installed for aesthetic purposes only. Memory addresses from the CP bus or the Memory Address switches are latched in this register.

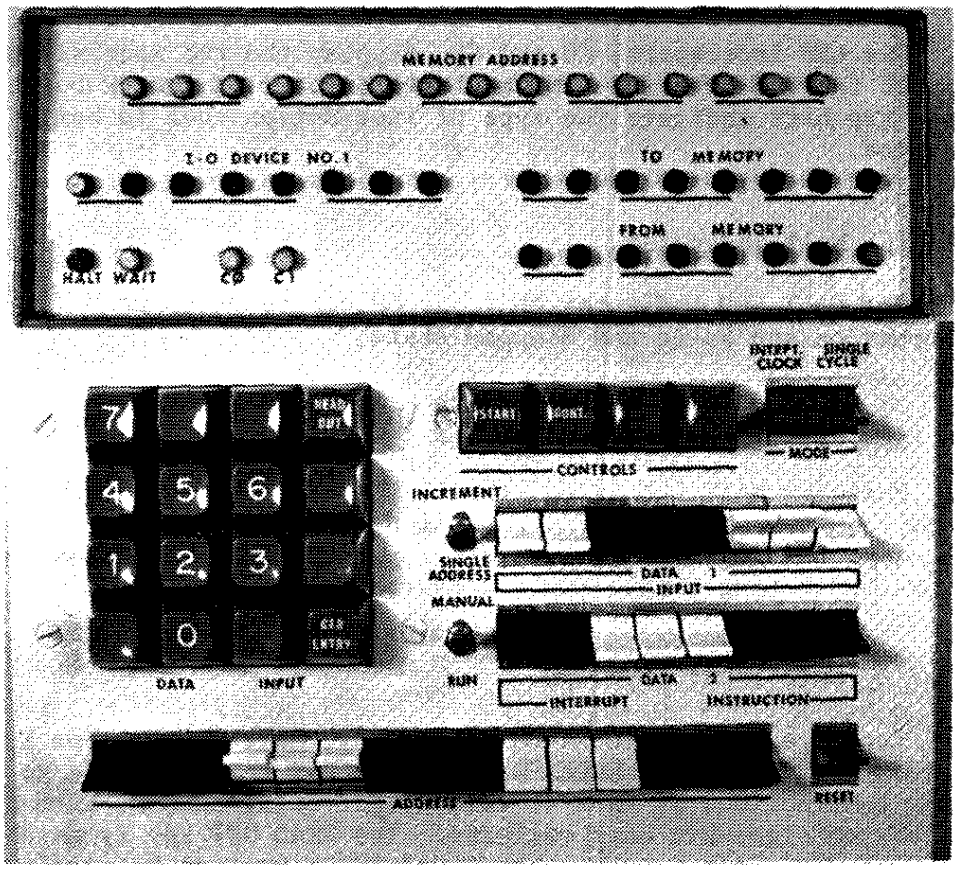


FIGURE 3-1. Microcomputer Controls And Display

III.1.2 To Memory Indicators

The To Memory indicators are a group of eight LED indicators, which display data that are presented to the RAM from the input keyboard.

III.1.3 From Memory Indicators

The From Memory indicators are a group of eight LED indicators, which display data that have been entered and read out by the keys.

III.1.4 I/O Device No. 1 Register

A one-byte (eight-bit) latching register stores output data during execution of OUT1 instruction.

III.1.5 Control Bits Indicators

Two LED indicators, C0 and C1, display the two most significant bits of the two-byte (16-bit) register/counter on the CP bus output. These two bits indicate the type of instruction that is being executed.

III.1.6 Halt Indicator

The HALT LED indicates that the CP has received an HLT instruction and is in the Stopped state.

III.1.7 Wait Indicator

When the WAIT LED is on, the CP is in its Pause, or Wait, state and is awaiting a true condition on the Ready (RDY) input line (Appendix A, Section A.3). This is the state in which the CP "waits" during Single Cycle operations.

III.1.8 Data Input Keyboard

Ten keys are operative on the 16-key, Hall-effect type keyboard: 0-7, READ OUT, CLEAR ENTRY. The 0-7 keys are used to enter instructions or data as three-digit octal numbers into the RAM via an eight-bit data register. The READ OUT key is used to read out data from memory. The CLEAR ENTRY key can be used to clear the data register, if a mistake has been made while keying in the first two (most significant) octal digits of data.

III.1.9 Memory Adress Switches

The starting address in a sequence of memory locations to be deposited into or to be examined is set up with the 15 MEMORY ADDRESS switches. The most significant digit switch is inoperative and is installed for aesthetic purposes only.

III.1.10 Interrupt Instruction Switches

A single-byte instruction that will be sent to the CP during a program interrupt cycle is set up on the eight interrupt/instruction switches. These switches are read during a CP startup to enter an initial restart (RST) instruction.

III.1.11 Input Data Switches

Eight Input Data switches are read into the CP accumulator during execution of INP1 instruction.

III.1.12 Control Push Buttons

Two of four control push buttons are operative. The START button initiates a program interrupt CP cycle to start a program. The CONTINUE button is used to "single cycle" through the memory cycles of a program in the Single Cycle mode.

III.1.13 Mode Switches

Program interrupt requests are sent to the CP from an interrupt clock when the Interrupt Clock switch is in the up position. Down is the normal operating position for the Single Cycle switch. When in up position, a program can be single-cycled with the CONTINUE key.

III.1.14 Manual Switch

With the MANUAL switch (a bat-handled toggle) in the up position, data can be entered into the memory from the DATA INPUT keyboard, or the memory contents can be examined by depressing the READ OUT key. Down position, RUN, is normal operation when a program is being executed.

III.1.15 Increment Switch

This toggle switch selects the SINGLE ADDRESS or INCREMENT mode for data key entry and memory data examining operations. In

the SINGLE ADDRESS mode, the address is not incremented during the keying operations. In the INCREMENT mode, the address is incremented automatically after having been deposited with data or examined.

III.1.16 Reset Switch

The RESET switch is depressed to clear the MEMORY ADDRESS and the TO MEMORY register.

III.1.17 I/O Connector

This 36-pin connector on the rear of the microcomputer chassis is used to connect an external device.

III.2 OPERATING PROCEDURES

III.2.1 General

The microcomputer may be operated as described in the next four sections. The operating instructions given are very general and do not describe the only methods of operation.

III.2.2 Program Operate Mode

To operate a program in the Desk-Top Microcomputer, the following procedure may be followed (assuming the PROM has been previously programmed and contains the desired programs to be run):

1. Turn on the AC power. The CP automatically goes through an internal procedure to clear its registers, then stops in the HALT state (HALT indicator should be on).

2. Set Manual/Run switch to RUN. Set both mode switches to down position.

3. Refer to Appendix A, Section A.4. Set the Interrupt/Instruction switches with an RST instruction to start the machine with a routine stored in PROM address 000, 010, 020, 030, 040, 050, 060, or 070 (see Table 3-1 for Memory Allocations).

TABLE 3-1. MICROCOMPUTER MEMORY ALLOCATIONS

Memory Type	Octal Address	Circuit Status
PROM	000-377 400-777 1000-1377 1400-1777	Can be directly plugged into 24-pin IC sockets (256 x 8 bits per module).
	2000-2377 2400-2777 3000-3377 3400-3777	Decoding logic provided (reserved for future circuit expansion).
RAM	4000-5777 6000-7777	Can be directly plugged into 16-pin IC sockets (8 sockets per 1K x 8 RAM).
	10000-11777 12000-13777	Decoding logic provided (reserved for future circuit expansion).
PROM, ROM, or RAM	14000-37777	Additional locations that can be accessed by Central Processor.

4. Depress START button. The program will be executed, starting at the PROM address specified in the RST instruction.

5. To stop program, set an HLT instruction on the Interrupt/Instruction switches. Depress START key.

6. To continue with the next instruction in sequence after HLT, set a NOP (no operation) instruction* on the Interrupt/Instruction switches. Depress START key.

7. When the program Interrupt Clock is turned on,interrupt signals are executed at the rate of the clock frequency (hardware controlled).. This operation is similar to continuously depressing the START key; therefore, the desired interrupt instruction must be set on the Interrupt Instruction Switches.

*The octal code for an NOP instruction is 300.

III.2.3 Single Cycle Mode

For program debugging or hardware maintenance purposes, a program may be "single cycled" so that registers can be examined during the execution sequence. The following procedure will operate the processor in that mode:

1. Follow procedures 1 to 3 in Section III.2.2.

2. Switch to SINGLE CYCLE mode.

3. Depress START key. Computer will execute the first instruction (normally a single-cycle RST instruction) and stop in the WAIT state (WAIT indicator on).

4. Depress SINGLE CYCLE key. The first cycle* of the next instruction will be executed, and the processor will again stop in the WAIT state.

5. Continue to depress SINGLE CYCLE key to step through the program.

6. At any place in the program, press the SINGLE CYCLE switch down to return to normal continuous operate mode.

III.2.4 Data Input Mode

The following procedure may be followed to enter data into the RAM or to examine the contents of the PROM or RAM:

1. With the machine in the HALT state, depress RESET.

2. If a sequence of addresses is to be loaded with data or examined, switch the control switch to Increment. During each deposit or examine operation, the address register will be incremented.

3. Set the Manual/Run Switch to MANUAL.

4. Select the address (or starting address in a sequence) with the Memory Address switches.

5. To deposit information into memory, simply key-in the information as a three-digit octal number (the most significant digit first). For example, to enter all

---

* An instruction may require from one to three cycles to complete its operation (see Reference 20, p. 16).

"1's" in a location, depress keys 3, 7, 7. After that operation, "377" should be displayed on the To Memory and From Memory registers. The address in which the number was deposited will be displayed on the Memory Address register. Enter the next datum, if operating in the Increment mode.

6. If a mistake is made while entering the first two digits, depress CLEAR ENTRY and key-in the corrected number.

7. To read out information in the PROM or RAM, follow steps 1 to 4 above, then depress the READ OUT key.

III.3 PROGRAMMING PROCEDURES

Routine test programs, startup programs, common subroutines, etc., may be permanently stored in four 256 x 8-bit PROMs (Model 1702A modules) and plugged into 24-pin module locations (C1-1, C1-2, C2-1, C2-2, Figure 2-5). Programs may be changed by re-programming* the PROM or by exchanging PROM modules. For program development, instructions can be easily entered, examined, and altered in the RAM, using the data input keyboard methods.

The Desk-Top Microcomputer is programmed in machine language. Appendix A, Section A.4 lists the basic instruction set for the Model 8008 CP and contains a minimum of information needed to write simple programs for the microcomputer. The user should be thoroughly familiar with the operation of the Model 8008 CP and programming methods before attempting to write more complicated programs. Many short and simple programs were written during the testing of the microcomputer; several typical programs are listed and described in Appendix B.

The special I/O instructions for this microcomputer and the associated process simulation chassis are defined in Table 3-2. The microcomputer has decoding logic to read-in four input devices and to output data to eight devices. These signals along with the CP data bus signals are wired to the I/O connector on the rear of the chassis. Additional logic could be added to provide more inputs and outputs.

A large number of single-pulse output functions, such as flip-flop clocks to turn relays, etc., on and off, clock pulses to operate

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* Specifications for the 1702A PROM and detailed discussions on programming and erasing the module are in Reference 21, page 3-7. A manual PROM programmer was fabricated during this study.

counters, sample-and-holds, multiplexers, and ADCs, can be generated by the microcomputer with a single output instruction. Hardware decodes the data on the CP bus at the time the instruction is issued.

TABLE 3-2. LIST OF SPECIAL INSTRUCTIONS

Mnemonic	Octal Instruction Code	Description of Operation
INP0	101	Read the ADC into the accumulator.
INP1	103	Read the Data 1 switches into the accumulator.
OUT0	161	Reset ADC and start next conversion.
OUT1	163	Write the content of the accumulator into the I/O Device No. 1 register.
OUT2	165	Write the content of the accumulator into the OUT-1 register on the Process Simulator chassis.
OUT3	167	Write the content of the accumulator into the OUT-2 register on the Process Simulator chassis.
OUT4	171	Send clock pulse input to the alarm flip-flops in the Process Simulator chassis.
OUT7	177	Clear the I/O Device No. 1 register.

IV. APPLICATIONS

IV.1. TRAINING AID

The Desk-Top Microcomputer, a miniature version of a general-purpose computer system, is inexpensive, easy to program, and easy to operate. The microcomputer could be applied most effectively to practical computer systems problems in an electronics laboratory.

A large computer system is covered up in complex peripherals, high level software, and complex operating procedures. Exposure to that type system often overwhelms a trainee to the extent that he cannot comprehend the fundamentals of the system. Using the microcomputer, fundamental design problems and maintenance techniques could be taught at the work bench level. The same techniques could then be applied more easily to the larger, more-complex systems.

IV.2 PROCESS CONTROL

The primary aim of this study was to design and develop microcomputer hardware; very little effort was expended on system software. A simple, but practical, program was written to demonstrate the microcomputer's ability to monitor and control a process. The program (Figure 4-1 and Appendix D) was stored in the PROM, beginning at address 70.

The first few steps in the program are to feed the initial data into the registers, to clear internal and I/O registers, and to set the memory registers for a temporary storage location in the RAM. The ADC data are then read into the accumulator* and displayed on the OUT-1 register and the analog meter on the simulator chassis. The ADC is reset, and a new conversion is initiated with the instruction OUT0. ADC data are then tested for a Hi Alarm condition.** If the ADC data are greater than the Hi Alarm setting, the Hi Alarm is turned on, and the program cycles back to program address 104 to read the ADC again.

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* ADC data are zero on the first pass through the program.

**Hi Alarm condition is set up with Data-1 Input switches on the console and can be changed while the program is operating.

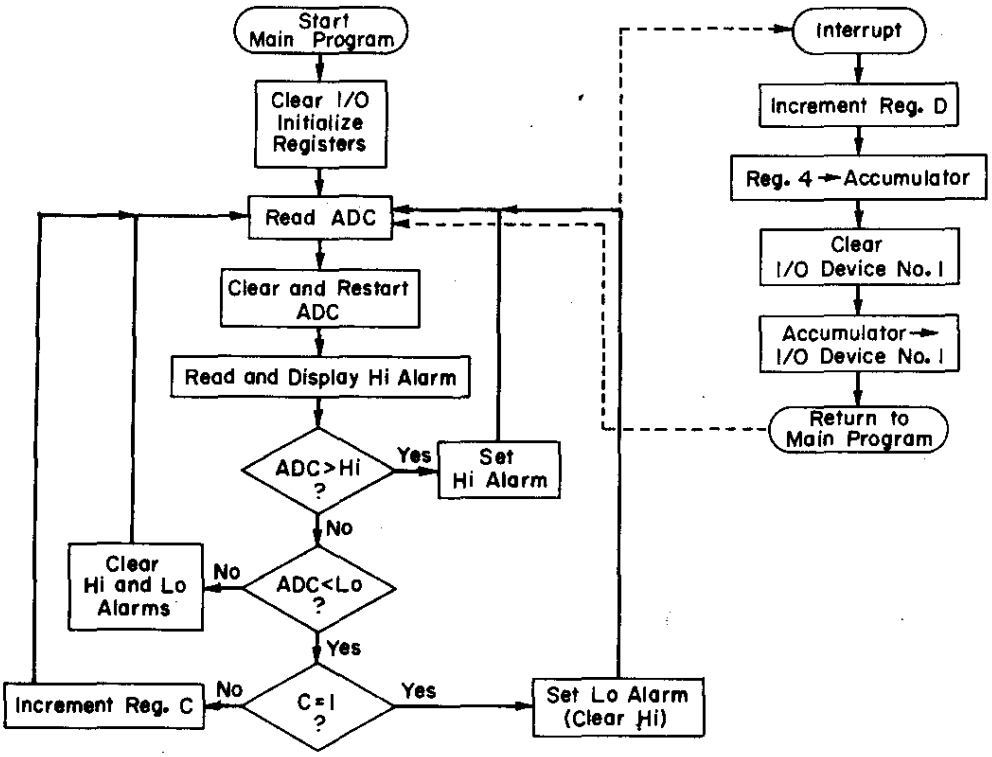

FIGURE 4-1. Control Program Flow Chart

If ADC data are less than or equal to Hi Alarm, ADC data are tested for Lo Alarm condition.* If Lo Alarm is greater than ADC reading, the program jumps to location 137 to test Register C for C = 1. Register C will equal zero on first pass only, so it will be incremented on the first pass. Program returns to location 104 to read new ADC value. If C = 1 in the above test, the Lo Alarm will be turned on, and the program will return to location 104. If Lo Alarm setting is less than or equal to ADC data, both Hi Alarm and Lo Alarm conditions are cleared, and the program returns to location 104.

An interrupt subroutine beginning at location 40 was written to increment I/O Device No. 1 display register on the control console each time an interrupt occurred. After the main control program has been initiated by RST instruction 075, the interrupt subroutine is started by setting the Interrupt/Instruction switches to 045 and then turning on the Interrupt Clock. After implementing the subroutine, the CP returns to where it left the main control program.

---

* Lo Alarm condition is set by software and is 1/8 of the full scale value in the program discussed.

The ADC has a maximum conversion time of 200 microseconds. In the main control program, ADC conversions are initiated at 300 to 500 microsecond intervals. Data to and from the process are transferred in eight-bit bytes. Using standard two's complement notation, bipolar data accuracy in the digital system would be ±0.8% full scale. Unipolar data would apply in many applications; accuracy would then be ±0.4% full scale.

IV.3 INTERFACING TECHNIQUES

The INP instructions of the CP instruction set provide reading in an eight-bit data word from one of eight addressable locations. The data words must be multiplexed to the CP data bus with appropriate external logic. Up to 256 data sources may be read into the CP with each of the eight possible INP instructions, if the external input logic is designed to use this "bonus" feature of the CP operation. When INP is executed, the CP accumulator data (Register A) are latched into the external 74197 modules with LO ADDR(L) during T1 state. During T2 state, the INP instruction word is latched into the register with HI ADDR(L). These data contain the binary address (DR9-DR11) and are decoded for the eight possible INP instructions. If an eight-bit address is loaded into the accumulator prior to executing an INP instruction, DR0-DR7 can be externally decoded during T1 state to give 256 additional address combinations for each INP instruction. As many as 2048 input devices may be addressed and read into Model 8008 CP. Although it is called an input instruction, INP pulses could be used as output pulses to trigger flip-flops for control alarms, indicators, process valves, etc.

The OUT instructions are executed exactly as INP except that states T4 and T5 are missing. T5 is used by INP to read in the eight-bit external data word. During T2, 24 devices may be addressed with separate OUT instructions. By decoding DR0-DR7, 256 additional address combinations are available for each OUT instruction. If one OUT instruction were designated to strobe an eight-bit data word to an external device, an additional OUT instruction could be used to send the data to any one of 5888 external devices.

Operating a process with an 8008 CP servicing 2048 inputs and 5888 outputs is not recommended. However, if two-byte (16-bit) transfers are desirable to get better accuracy, a few of the extra INP and OUT instructions may be useful.

An additional interfacing design feature that was not used by the Desk-Top Microcomputer is the decoding and outputing of four CP condition flip-flops (S, Z, P, C) during an INP instruction.[20] These flags on DR0-DR3 at T4 state may be used for conditional I/O transfers. The Model 8008 CP has extremely powerful I/O capabilities.

V. CONCLUSIONS

The Desk-Top Microcomputer has demonstrated that it is both feasible and practical to use microcomputers in educational and process control applications. Actually, microcomputers are already appearing in many other application areas.[30] It is evident by the dates of the publications in the Reference section of this report, that this is a new area of work in electronic engineering (all reference material that could be assembled was published during the duration of this project).

The engineer must become more "systems oriented" in his approach to a design problem. He also must become more involved in computer systems software and will be required, in many applications, to write programs at the machine language level.[25] Not only will engineers soon be using these modules in system designs, they may be using a microcomputer to design and develop digital systems.[26]

Although the present microcomputers have not presented a serious threat to minicomputer systems, due primarily to limitations in speed and software,[19] strong indications are that microprocessors to be introduced within a year may do just that.[27] In many applications microcomputers already have the capability and the low price tag to replace basic minicomputers.[28] Microcomputer applications were a main topic at the Wescon Show in San Francisco, September 1973.[29]

Microcomputers already have the specifications required to do most process control and data logging. The eight-bit data word gives better than 1% accuracy and data sample rates can be easily satisfied for many routine systems. Double-precision (16-bit) data words could be implemented for many processes that have low sample rate requirements. A system could be designed in a hierarchy configuration using a large number of microprocessors dedicated to simple tasks and being controlled by a more-sophisticated supervisory system. Many hardwired digital systems could be replaced with microprocessors and firmware.[31] One company has introduced a line of digital logic plug-in modules incorporating an LSI CP module and associated circuits, and the user can purchase a microprocessor system as a "do-it-yourself" kit.[32]

This study revealed the usefulness of the new LSI modules; however, it also revealed the difficult mechanical and electronic problems that are involved in the over-all design and fabrication of a system using these modules. The maintenance of these sophisticated electronics systems will require highly skilled electronic technicians.

VI. ACKNOWLEDGMENT

The material in this report was accepted in partial fulfillment of the requirements for the Degree of Master of Science in Electrical Engineering at the University of South Carolina, Columbia, South Carolina, December 1973.

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APPENDIX A. THE CENTRAL PROCESSOR

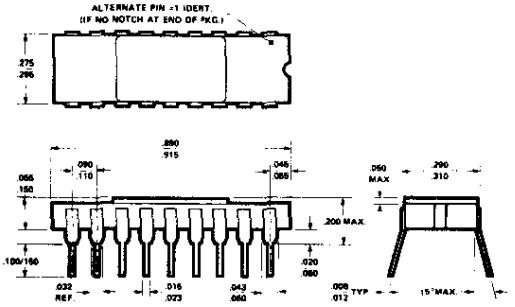
The CP module used in this design was the Intel Model 8008. It was selected due to its proven reliability and availability, low cost, and single 16-pin DIP module feature. The manufacturer's users manual[20] contains complete documentation necessary for a thorough understanding of its operation. Tables and diagrams pertinent to the circuit design in this report have been excerpted from that reference and appear in this appendix.

The Model 8008 is a complete, single-chip, 8-bit, parallel computer CP that can directly access up to 16k bytes (8 bits) of memory. It contains the arithmetic unit, eight 8-bit general-purpose registers, an 8 x 14-bit stack, and an 8-bit input/output data bus. Its inputs are TTL compatible; its outputs are low-level TTL compatible. It operates from a 500 kHz clock and has a hardware program interrupt feature. Its basic 48 instruction repertoire has useful combinations of index register operations, accumulator group, program counter and stack control, input/output, and machine instructions. Typical instructions are one to three bytes in length requiring 20 to 60 microseconds for execution. Instruction phase STATE and SYNC signals are provided for flexible interfacing.

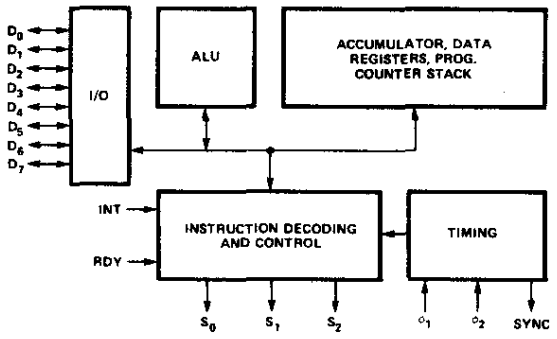
A.1. 8008 Physical Specifications (from Ref. 20)

Packaging Information

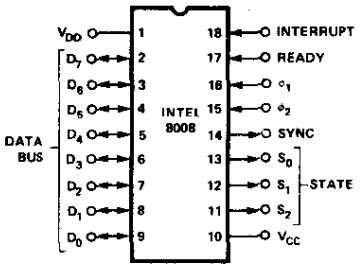
CERAMIC PACKAGE OUTLINE



BLOCK DIAGRAM



PIN CONFIGURATION



A.2. 8008 Electrical Specifications (from Ref. 20)

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−55°C to +150°C
Input Voltages and Supply Voltage With Respect to V_{CC}	+0.5 to −20V
Power Dissipation	1.0 W @ 25°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

D.C. AND OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = +5V ±5%, V_{DD} = −9V ±5% unless otherwise specified. Logic "1" is defined as the more positive level (V_{IH}, V_{OH}). Logic "0" is defined as the more negative level (V_{IL}, V_{OL}).

SYMBOL	PARAMETER	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
I_{DD}	AVERAGE SUPPLY CURRENT - OUTPUTS LOADED*		30	60	mA	T_A = 25°C
I_{LI}	INPUT LEAKAGE CURRENT			10	μA	V_{IN} = 0V
V_{IL}	INPUT LOW VOLTAGE (INCLUDING CLOCKS)	V_{DD}		V_{CC}−4.2	V	
V_{IH}	INPUT HIGH VOLTAGE (INCLUDING CLOCKS)	V_{CC}−1.5		V_{CC}+0.3	V	
V_{OL}	OUTPUT LOW VOLTAGE			0.4	V	I_{OL} = 0.44mA C_L = 200 pF
V_{OH}	OUTPUT HIGH VOLTAGE	V_{CC}−1.5			V	I_{OH} = 0.2mA

*Measurements are made while the 8008 is executing a typical sequence of instructions. The test load is selected such that at V_{OL} = 0.4V, I_{OL} = 0.44mA on each output.

A.C. CHARACTERISTICS

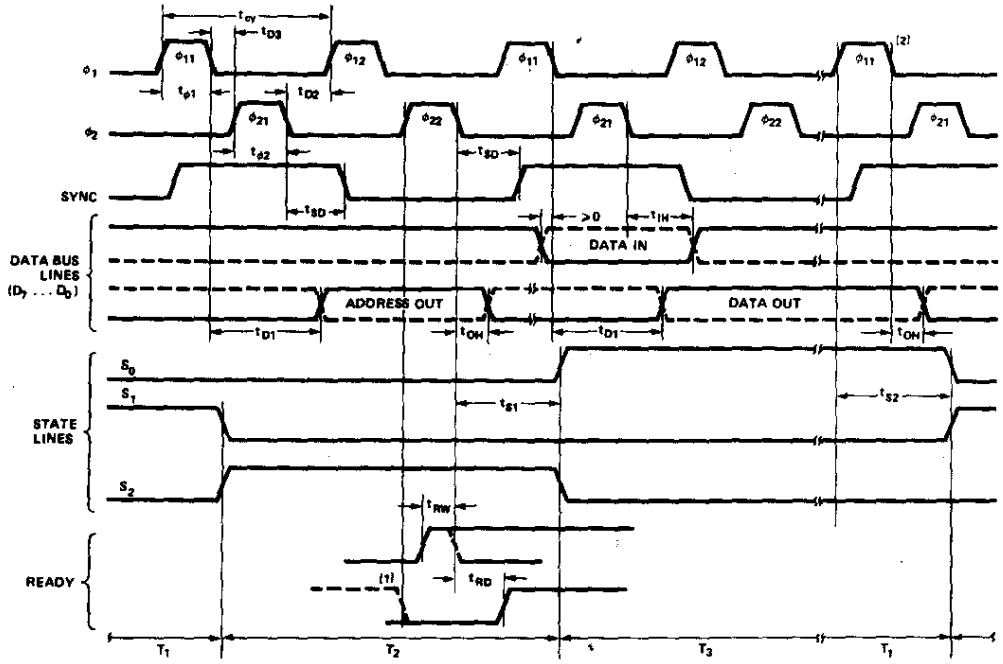
T_A = 0°C to 70°C; V_{CC} = +5V ±5%, V_{DD} = −9V ±5%. All measurements are referenced to 1.5V levels.

SYMBOL	PARAMETER	8008 LIMITS MIN.	8008 LIMITS MAX.	8008-1 LIMITS MIN.	8008-1 LIMITS MAX.	UNIT	TEST CONDITIONS
t_{CY}	CLOCK PERIOD	2	3	1.25	3	μs	t_R,t_F = 50ns
t_R,t_F	CLOCK RISE AND FALL TIMES		50		50	ns	
$t_{\phi 1}$	PULSE WIDTH OF ϕ_1	.70		.35		μs	
$t_{\phi 2}$	PULSE WIDTH OF ϕ_2	.55		.35		μs	
t_{D1}	CLOCK DELAY FROM FALLING EDGE OF ϕ_1 TO FALLING EDGE OF ϕ_2	.90	1.1		1.1	μs	
t_{D2}	CLOCK DELAY FROM ϕ_2 TO ϕ_1	.40		.35		μs	
t_{D3}	CLOCK DELAY FROM ϕ_1 TO ϕ_2	.20		.20		μs	
t_{DD}	DATA OUT DELAY		1.0		1.0	μs	C_L = 100pF
t_{OH}	HOLD TIME FOR DATA BUS OUT	.10		.10		μs	
t_{IH}	HOLD TIME FOR DATA IN	[1]		[1]		μs	
t_{SD}	SYNC OUT DELAY		.70		.70	μs	C_L = 100pF
t_{S1}	STATE OUT DELAY (ALL STATES EXCEPT T1 AND T1I) [2]		1.1		1.1	μs	C_L = 100pF
t_{S2}	STATE OUT DELAY (STATES T1 AND T1I)		1.0		1.0	μs	C_L = 100pF
t_{RW}	PULSE WIDTH OF READY DURING ϕ_{22} TO ENTER T3 STATE	.35		.35		μs	
t_{RD}	READY DELAY TO ENTER WAIT STATE	.20		.20		μs	

[1] t_{IH} MIN ≥ t_{SD}

[2] If the INTERRUPT is not used, all states have the same output delay, t_{S1}.

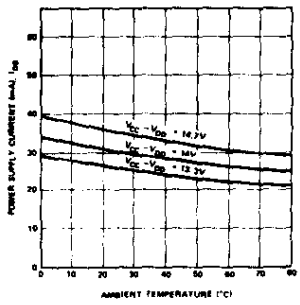
TIMING DIAGRAM



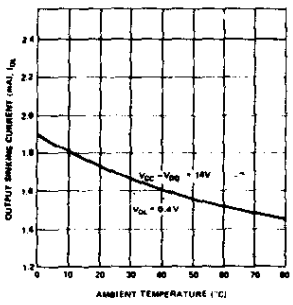
[1] READY line must be at "0" prior to ϕ_{22} of T_2 to guarantee entry into the WAIT state.
[2] INTERRUPT line must not change levels within 200ns (max.) of the falling edge of ϕ_1.

TYPICAL D.C. CHARACTERISTICS

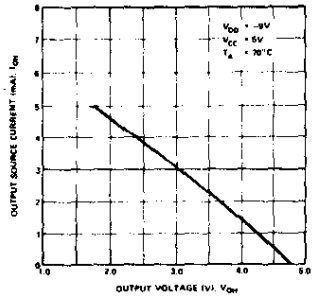
POWER SUPPLY CURRENT VS. TEMPERATURE



OUTPUT SINKING CURRENT VS. TEMPERATURE

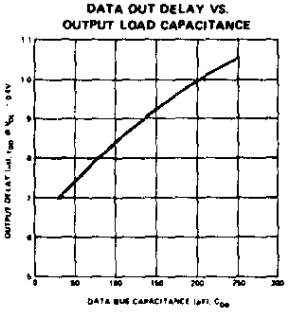


OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



TYPICAL A.C. CHARACTERISTICS

DATA OUT DELAY VS. OUTPUT LOAD CAPACITANCE



CAPACITANCE f = 1MHz; T_A = 25°C; Unmeasured Pins Grounded

SYMBOL	TEST	LIMIT (pF)	
		TYP.	MAX.
C_{IN}	INPUT CAPACITANCE	5	10
C_{DB}	DATA BUS I/O CAPACITANCE	5	10
C_{OUT}	OUTPUT CAPACITANCE	5	10

A.3. 8008 Timing Diagrams (from Ref. 20)

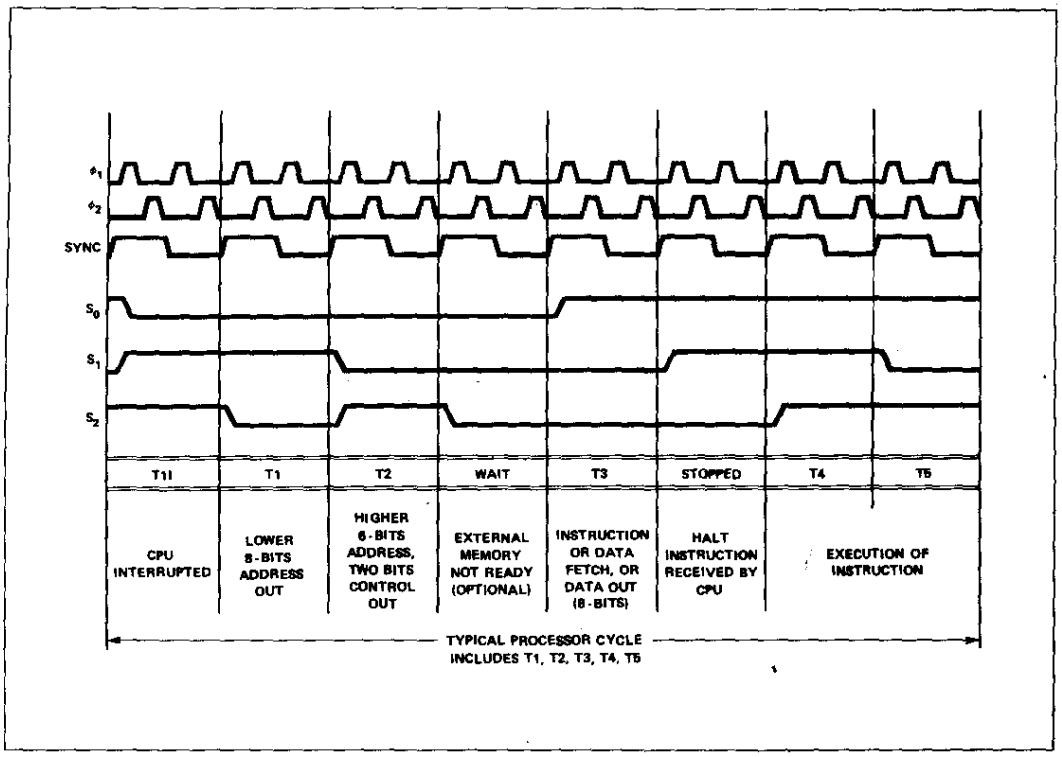


Figure 1. Basic 8008 Instruction Cycle

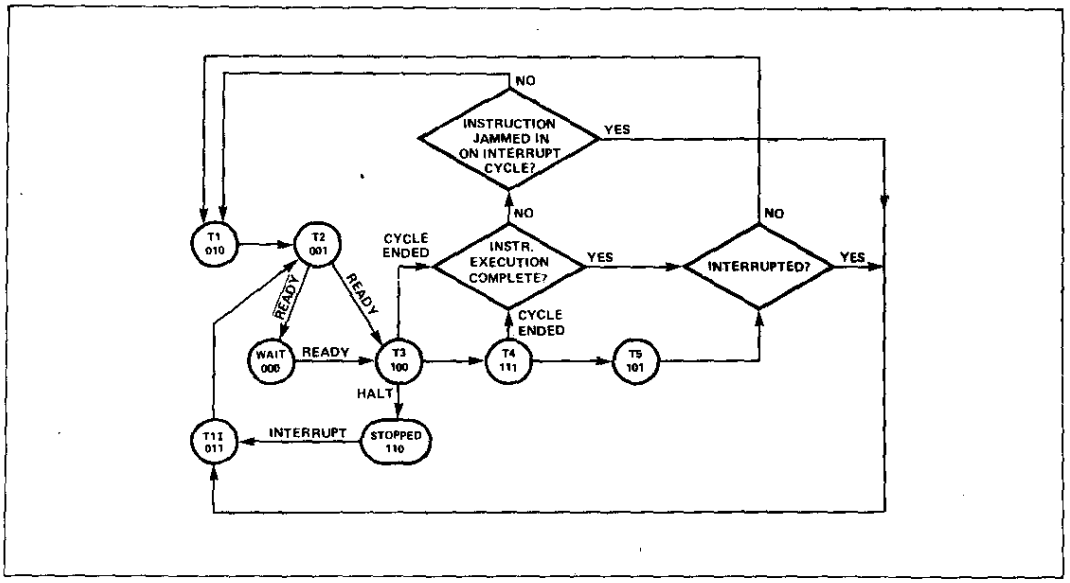


Figure 2. CPU State Transition Diagram

A.4. 8008 Instruction Set (from Ref. 20)

IV. BASIC INSTRUCTION SET

The following section presents the basic instruction set of the 8008.

A. Data and Instruction Formats

Data in the 8008 is stored in the form of 8-bit binary integers. All data transfers to the system data bus will be in the same format.

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

DATA WORD

The program instructions may be one, two, or three bytes in length. Multiple byte instructions must be stored in successive words in program memory. The instruction formats then depend on the particular operation executed.

		TYPICAL INSTRUCTIONS
One Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	Register to register, memory reference, I/O arithmetic or logical, rotate or return instructions
Two Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OPERAND	Immediate mode instructions
Three Byte Instructions		
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	OP CODE	
D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	LOW ADDRESS	JUMP or CALL instructions
X X D_5 D_4 D_3 D_2 D_1 D_0	HIGH ADDRESS*	*For the third byte of this instruction, D_6 and D_7 are "don't care" bits.

For the MCS-8 a logic "1" is defined as a high level and a logic "0" is defined as a low level.

B. Summary of Processor Instructions

Index Register Instructions

The load instructions do not affect the flag flip-flops. The increment and decrement instructions affect all flip-flops except the carry.

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE D_7 D_6	D_5 D_4 D_3	D_2 D_1 D_0	DESCRIPTION OF OPERATION
(1) Lr_1r_2	(5)	1 1	D D D	S S S	Load index register r_1 with the content of index register r_2.
(2) LrM	(8)	1 1	D D D	1 1 1	Load index register r with the content of memory register M.
LMr	(7)	1 1	1 1 1	S S S	Load memory register M with the content of index register r.
(3) Lri	(8)	0 0 B B	D D D B B B	1 1 0 B B B	Load index register r with data B . . . B.
LMI	(9)	0 0 B B	1 1 1 B B B	1 1 0 B B B	Load memory register M with data B . . . B.
INr	(5)	0 0	D D D	0 0 0	Increment the content of index register r (r ≠ A).
DCr	(5)	0 0	D D D	0 0 1	Decrement the content of index register r (r ≠ A).

Accumulator Group Instructions

The result of the ALU instructions affect all of the flag flip-flops. The rotate instructions affect only the carry flip-flop.

ADr	(5)	1 0	0 0 0	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator. An overflow (carry) sets the carry flip-flop.
ADM	(8)	1 0	0 0 0	1 1 1	
ADI	(8)	0 0 B B	0 0 0 B B B	1 0 0 B B B	
ACr	(5)	1 0	0 0 1	S S S	Add the content of index register r, memory register M, or data B . . . B to the accumulator with carry. An overflow (carry) sets the carry flip-flop.
ACM	(8)	1 0	0 0 1	1 1 1	
ACI	(8)	0 0 B B	0 0 1 B B B	1 0 0 B B B	
SUr	(5)	1 0	0 1 0	S S S	Subtract the content of index register r, memory register M, or data B . . . B from the accumulator. An underflow (borrow) sets the carry flip-flop.
SUM	(8)	1 0	0 1 0	1 1 1	
SUI	(8)	0 0 B B	0 1 0 B B B	1 0 0 B B B	
SBr	(5)	1 0	0 1 1	S S S	Subtract the content of index register r, memory register M, or data data B . . . B from the accumulator with borrow. An underflow (borrow) sets the carry flip-flop.
SBM	(8)	1 0	0 1 1	1 1 1	
SBI	(8)	0 0 B B	0 1 1 B B B	1 0 0 B B B	

MNEMONIC	MINIMUM STATES REQUIRED	INSTRUCTION CODE $D_7 D_6$	$D_5 D_4 D_3$	$D_2 D_1 D_0$	DESCRIPTION OF OPERATION
NDr	(5)	1 0	1 0 0	S S S	Compute the logical AND of the content of index register r, memory register M, or data B . . . B with the accumulator.
NDM	(8)	1 0	1 0 0	1 1 1	
NDI	(8)	0 0 B B	1 0 0 B B B	1 0 0 B B B	
XRr	(5)	1 0	1 0 1	S S S	Compute the EXCLUSIVE OR of the content of index register r, memory register M, or data B . . . B with the accumulator.
XRM	(8)	1 0	1 0 1	1 1 1	
XRI	(8)	0 0 B B	1 0 1 B B B	1 0 0 B B B	
ORr	(5)	1 0	1 1 0	S S S	Compute the INCLUSIVE OR of the content of index register r, memory register m, or data B . . . B with the accumulator.
ORM	(8)	1 0	1 1 0	1 1 1	
ORI	(8)	0 0 B B	1 1 0 B B B	1 0 0 B B B	
CPr	(5)	1 0	1 1 1	S S S	Compare the content of index register r, memory register M, or data B . . . B with the accumulator. The content of the accumulator is unchanged.
CPM	(8)	1 0	1 1 1	1 1 1	
CPI	(8)	0 0 B B	1 1 1 B B B	1 0 0 B B B	
RLC	(5)	0 0	0 0 0	0 1 0	Rotate the content of the accumulator left.
RRC	(5)	0 0	0 0 1	0 1 0	Rotate the content of the accumulator right.
RAL	(5)	0 0	0 1 0	0 1 0	Rotate the content of the accumulator left through the carry.
RAR	(5)	0 0	0 1 1	0 1 0	Rotate the content of the accumulator right through the carry.

Program Counter and Stack Control Instructions

(4) JMP	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$.
(5) JFc	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
JTc	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 0 0 B_2 B_2 B_2 B_3 B_3 B_3	Jump to memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
CAL	(11)	0 1 B_2 B_2 X X	X X X B_2 B_2 B_2 B_3 B_3 B_3	1 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Unconditionally call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$. Save the current address (up one level in the stack).
CFc	(9 or 11)	0 1 B_2 B_2 X X	0 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop c is false, and save the current address (up one level in the stack.) Otherwise, execute the next instruction in sequence.
CTc	(9 or 11)	0 1 B_2 B_2 X X	1 C_4 C_3 B_2 B_2 B_2 B_3 B_3 B_3	0 1 0 B_2 B_2 B_2 B_3 B_3 B_3	Call the subroutine at memory address $B_3 \ldots B_3B_2 \ldots B_2$ if the condition flip-flop c is true, and save the current address (up one level in the stack). Otherwise, execute the next instruction in sequence.
RET	(5)	0 0	X X X	1 1 1	Unconditionally return (down one level in the stack).
RFc	(3 or 5)	0 0	0 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop c is false. Otherwise, execute the next instruction in sequence.
RTc	(3 or 5)	0 0	1 C_4 C_3	0 1 1	Return (down one level in the stack) if the condition flip-flop c is true. Otherwise, execute the next instruction in sequence.
RST	(5)	0 0	A A A	1 0 1	Call the subroutine at memory address AAA000 (up one level in the stack).

Input/Output Instructions

INP	(8)	0 1	0 0 M	M M 1	Read the content of the selected input port (MMM) into the accumulator.
OUT	(6)	0 1	R R M	M M 1	Write the content of the accumulator into the selected output port (RRMMM, RR ≠ 00).

Machine Instruction

HLT	(4)	0 0	0 0 0	0 0 X	Enter the STOPPED state and remain there until interrupted.
HLT	(4)	1 1	1 1 1	1 1 1	Enter the STOPPED state and remain there until interrupted.

NOTES:

(1) SSS = Source Index Register, DDD = Destination Index Register. These registers, r_i, are designated A(accumulator–000), B(001), C(010), D(011), E(100), H(101), L(110).

(2) Memory registers are addressed by the contents of registers H & L.

(3) Additional bytes of instruction are designated by BBBBBBBB.

(4) X = "Don't Care".

(5) Flag flip-flops are defined by C_4C_3: carry (00-overflow or underflow), zero (01-result is zero), sign (10-MSB of result is "1"), parity (11-parity is even).

APPENDIX B. TEST PROGRAMS

B.1 Read Data-1 Switches on Console and Display on Lights.

Address	Instruction Nmemonic	Octal	Description of Operation
4000/	INP1	103	Read data from switches
	OUT1	163	Display data
	JMP	104 000 010	Jump to 4000

B.2 Increment I/O Register (on Console) Until all 1's then Halt. Repeat when Program is Continued.

4100/	Lr_1I	016 000	Clear Register B
	Lr_0r_1	301	Load accum. with reg. B
	CPI	074 377	Set accum. to 377
	CT_c	152 113 010	If result of above subtraction is 0, call subroutine at 4113
	JMP	104 100 010	Jump to 4100
4113/	HLT[a]	377	Halt
	RET	007	Return to main program

---

a. Program halts. To continue, set Interrupt/Instruction switches to NOP (300) and depress START key.

B.3 Add Two Three Digit Octal Numbers. Display Result on Console I/O Register. Key in Octal Numbers at 5020 and 5021. Start Program at 5000.

5000/	Lr_6I	066 020	Set Memory Address to 5020
	Lr_5I	056 012	
	Lr_0M	307	Load accum. with 5020
	INr_6	060	Increment reg. L
	ADM	207	Accum. + 5021
	OUT1	163	Display result
	HLT	377	Halt

B.4 Shift a Bit Left and Right in Console I/O Display. Shift Speed Controlled with Console Data-1 Switches (000 is Setting for Fastest Shift Speed).

4000/	Lr_4I	046 000	Clear reg. E
	Lr_6I	066 200	M = 4200
	Lr_5I	056 010	
	Lr_0I	006 001	A = 1
	Lr_1r_0	310	Reg. B = 1
	Lr_2I	026 200	Reg. C = 200
4013/	OUT1	163	Display A
	RLC	002	Rotate A left
	CAL	106 043 010	Call DELAY

		CPr_2	272	A = reg. C
		JT_{01}	150 027 010	If result is 0, jump to 4027
		JMP	104 013 010	Jump to 4013
	4027/	OUT1	163	Display A
		CAL	106 043 010	Call DELAY
		RRC	012	Rotate A right
		CPr_1	271	A = reg. B
		JT_{01}	150 013 010	If result is 0, jump to 4013
		JMP	104 027 010	Jump to 4027
DELAY	4043/	LMr_0	370	4200 = A
		INr_3	030	Increment reg. D
		Lr_0r_3	303	A = reg. D
		CPI	074 377	A = 377
		JF_{01}	110 044 010	If result not 0, jump to 4044
		INP1	103	Read switches
		INr_4	040	Increment reg. E
		CPr_4	274	A = reg. E
		JT_{10}	160 064 010	If result negative, skip next instruction

JF_{01}	110 044 010	If result not 0, jump to 4044
Lr_4I	046 000	Clear reg. E
Lr_0M	307	A = 4200
RET	007	Return

B.5 Demonstration Program

This program was written by R. J. Sand, Savannah River Laboratory. It is a demonstration program of the graphics capability of the microcomputer. X and Y inputs to an oscilloscope are connected to the BNC output connectors on the rear of the Process Simulator Chassis.

The display presented on the oscilloscope is an "expanding square."

PROGRAM LISTING

MAIN/5000/Lr_1I	016 177	Set B = 177
Lr_0r_1	301	A ← B
OUT2	165	X ← A
Lr_2I	026 177	Set C = 177
Lr_0r_2	302	A ← C
OUT3	167	Y ← A
5010/Lr_3I	036 001	Set D = 1
Lr_4I	046 000	Set E = 0
CAL	106 120 012	Call INC C 5120

INr_4	040	E = E + 1
5020/Lr_0r_4	304	A ← E
CPr_3	273	A - D
JF_{01}	110 014 012	If not zero jump to 5014
Lr_4I	046 000	E = 0
CAL	106	Call INC B 5110
5030/	110 012	
INr_4	040	E = E + 1
Lr_0r_4	304	A ← E
CPr_3	273	A - D
JF_{01}	110 027 012	If not zero jump to 5027
5040/Lr_4I	046 000	E = 0
INr_3	030	D = D + 1
CAL	106 124 012	Call DEC C 5124
INr_4	040	E = E + 1
Lr_0r_4	304	A ← E
5050/CPr_3	273	A - D
JF_{01}	110 043 012	If not zero jump to 5043
Lr_4I	046 000	E = 0

```
          CAL       106       Call DEC B 5114
                    114

     5060/          012

          INr4      040       E = E + 1

          Lr0r4     304       A ← E

          CPr3      273       A - D

          JF01      110       If not zero jump to 5056
                    056
                    012

          Lr4I      046       E = 0

     5070/          000

          INr3      030       D = D + 1

          Lr0r3     030       A ← D

          CPI       074       D - 377
                    377       Any odd number 377 max

          JT01      150       If zero jump to 5000
                    000
                    012

     5100/JMP       104       Jump to 5014
                    014
                    012

INCB/5110/INr1      010       B = B + 1

          Lr0r1     301       A ← B

          OUT2      165       X ← A

          RET       007       RETURN

DECB/     DCr1      011       B = B - 1

          Lr0r1     301       A ← B

          OUT2      165       X ← A

          RET       007       RETURN
```

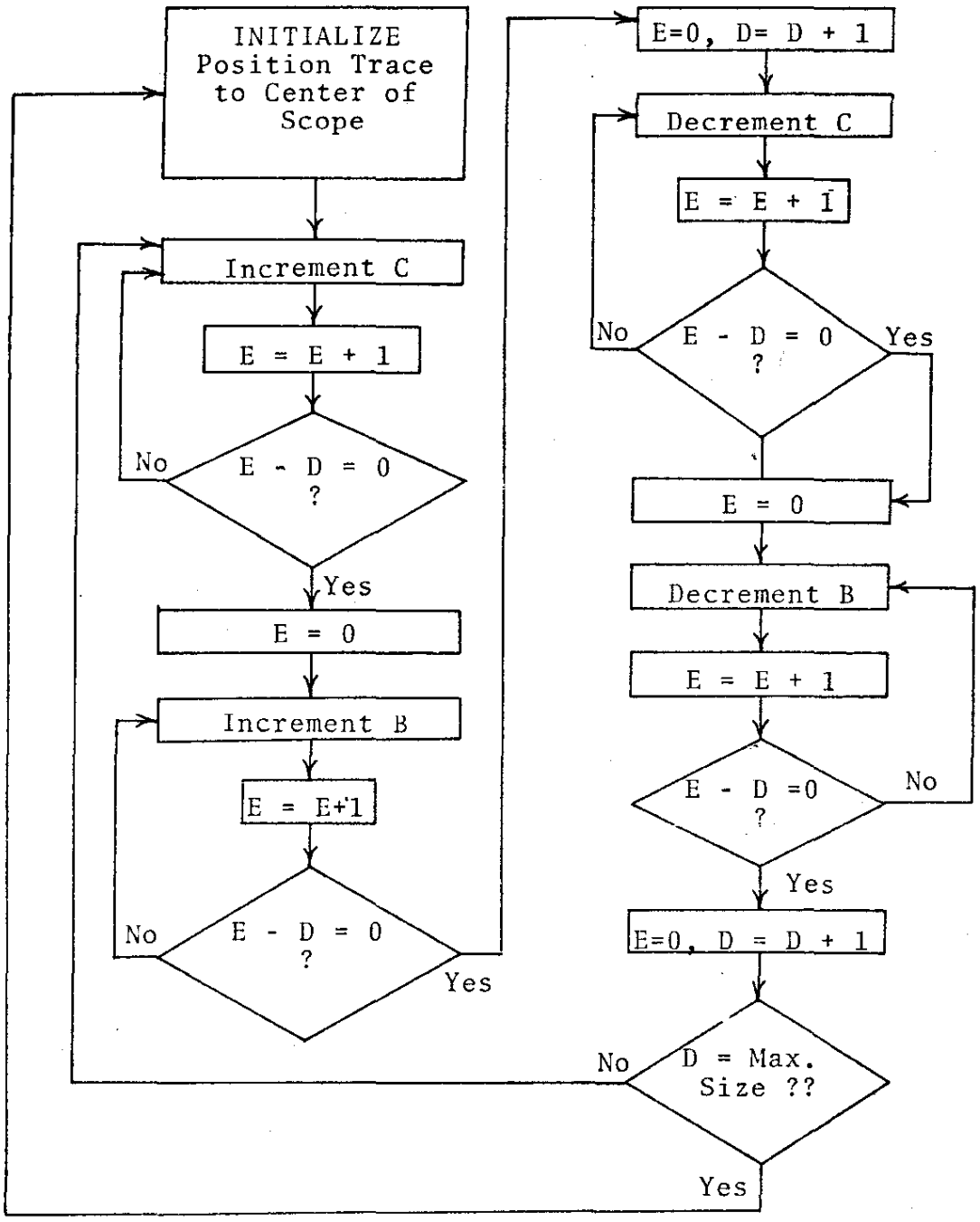
```
INCC/5120/INr2      020     C = C + 1
            Lr0r2   302     A ← C
            OUT3    167     Y ← A
            RET     007     RETURN
DECC/       DCr2    021     C = C - 1
            Lr0r2   302     A ← C
            OUT3    167     Y ← A
            RET     007     RETURN
```

RJS: 10/18/73

GRAPHICS CONTROL DEMONSTRATION

X-Y OSCILLOSCOPE CONTROL

Expanding Square



APPENDIX C. DATA SHEETS

This Appendix contains copies of data sheets for modules not contained in referenced material.

C.1. Oscillator Pin Connections and Specifications

Model No: 7404

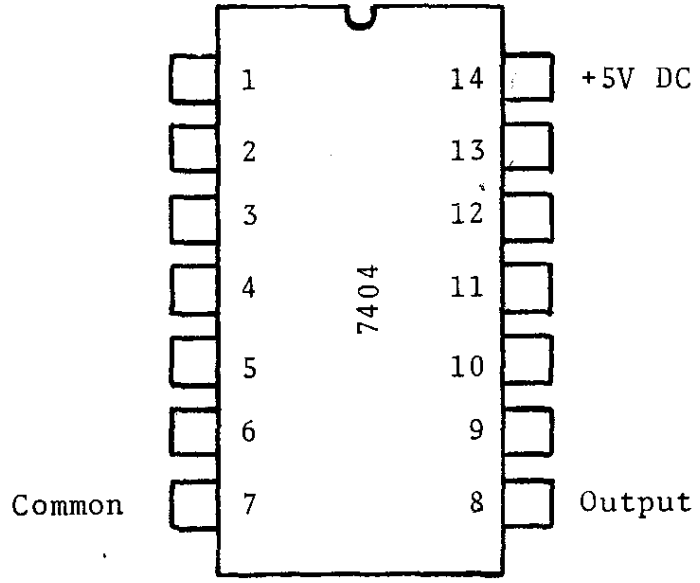
Input Power: +5V DC

Current: 35 ma max.

Output: 1.000 MHz, Square Wave, TTL compatible

Dimensions: 0.5 x 0.8 x 0.55 h, 14-pin DIP

Pin Connections



Manufactured by: Spectrum Technology, Inc.
P. O. Box 948
Galeta, CA 93017

C.2. HD-0165 Specification Sheet

HARRIS SEMICONDUCTOR

HD-

KEYBOARD ENCODER

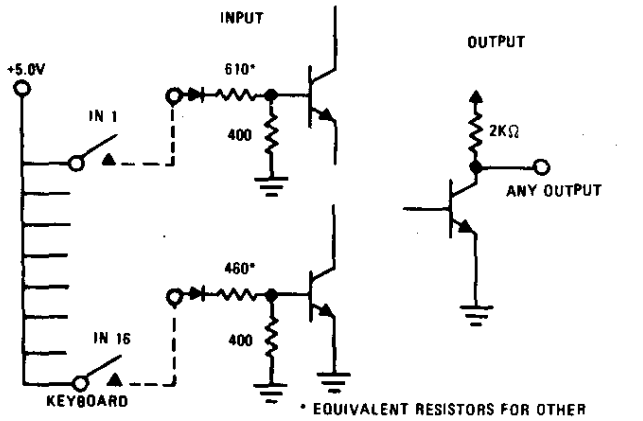
FEATURES

- STROBE OUTPUT
- KEY ROLLOVER OUTPUT
- EXPANDABLE: 2 PACKAGES REQUIRED FOR FULL TELETYPEWRITER, EIGHT-BIT ENCODING
- SINGLE +5.0V SUPPLY REQUIRED, DTL/TTL OUTPUTS
- MONOLITHIC RELIABILITY

GENERAL DESCRIPTION

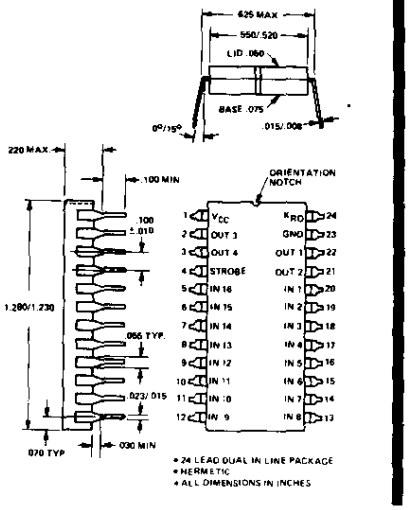
The HD-0165 Keyboard Encoder is a 16 line to four-bit parallel encoder intended for use with manual data entry devices such as calculator or typewriter keyboards. In addition to the encoding function, there is a Strobe output and a Key Rollover output which energizes whenever two or more inputs are energized simultaneously. Any four-bit code can be implemented by proper wiring of the input lines. Inputs are normally wired through the key switches to the +5.0V power supply. Full typewriter keyboard encoding up to eight bits can be accomplished with two Encoder circuits by the use of double pole key switches or single pole switches with two isolation diodes per key. Outputs will interface with all popular DTL and TTL logic families. The circuit is packaged in a hermetic 24-pin dual in-line package and operates over the temperature range of 0^{0}C to $+75^{0}$C.

EQUIVALENT CIRCUITS



* EQUIVALENT RESISTORS FOR OTHER INPUTS ARE BETWEEN THESE TWO VALUES

PACKAGE



* 24 LEAD DUAL IN LINE PACKAGE
* HERMETIC
* ALL DIMENSIONS IN INCHES

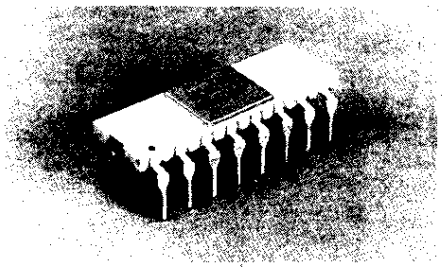
MK 5009 P

MOS Counter Time-Base Circuit

MOSTEK CORPORATION

DS-5009672-2 / AUG 1972

- ☐ Ion-implanted for full TTL/DTL compatibility
- ☐ Internal clock operates from:
  - External signal
  - External RC network
  - External crystal
- ☐ Operates DC to above 1 MHz
- ☐ Binary-encoded for frequency selection



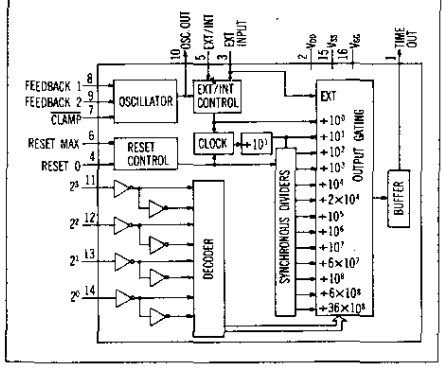
DESCRIPTION

The MK 5009 P is a highly versatile MOS oscillator and divider chain manufactured by Mostek using its depletion-load, ion-implantation process and P.-channel technology. The 16-pin DIP package provides frequency division ranges from 1 to 36×10^8. The circuit will operate from any of three frequency sources: the internal oscillator with an external RC combination; the internal oscillator with an external crystal; or with an externally-applied TTL signal. Control inputs provide additional versatility and allow the circuit to be used in a variety of applications including instruments, timers, and clocks.

With an input frequency of 1 MHz, the MK 5009 P provides the basic time periods necessary for most frequency measuring instruments, i.e., 1 μs through 100 seconds. One-minute, ten-minute, and one-hour periods are also available using a 1 MHz input. Using a 1/1.2 MHz input, the MK 5009 P can also provide a 50/60 Hz output for accurate generation of line frequencies in portable instruments or clocks.

The time-base output (TIME OUT) is a square wave, its frequency determined by the selected counter division, and by the oscillator frequency or external input. The falling edge of the output square wave should be used to control external gating circuitry.

FUNCTIONAL DIAGRAM



TIME OUT

ADDRESS INPUTS				WITHOUT RESET	RESET		BYPASS MODES (see page 3)		
					Reset Max.	Reset Min.	Mode 1	Mode 2	Mode 3
				$R_{MAX}=0$	$R_{MAX}=1$	$R_{MAX}=0$	$R_{MAX}=V_{SS}$	$R_{MAX}=0$	$R_{MAX}=V_{SS}$
2^3	2^2	2^1	2^0	$R_0=0$	$R_0=0$	$R_0=1$	$R_0=0$	$R_0=V_{SS}$	$R_0=V_{SS}$
0	0	0	0	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$	$\div 10^0$
0	0	0	1	$\div 10^1$			$\div 10^1$	$\div 10^1$	$\div 10^1$
0	0	1	0	$\div 10^2$	Resets	Resets	$\div 10^2$	$\div 10^2$	$\div 10^2$
0	0	1	1	$\div 10^3$			$\div 10^3$	$\div 10^3$	$\div 10^3$
0	1	0	0	$\div 10^4$	Counters	Counters	$\div 10^4$	$\div 10^4$	$\div 10^4$
0	1	0	1	$\div 10^5$			$\div 10^2$	$\div 10^5$	$\div 10^2$
0	1	1	0	$\div 10^6$	to their	to their	$\div 10^3$	$\div 10^6$	$\div 10^3$
0	1	1	1	$\div 10^7$			$\div 10^4$	$\div 10^7$	$\div 10^4$
1	0	0	0	$\div 10^8$	Highest	Lowest	$\div 10^5$	$\div 10^5$	$\div 10^2$
1	0	0	1	$\div 6\times10^7$			$\div 6\times10^4$	$\div 6\times10^4$	$\div 6\times10^1$
1	0	1	0	$\div 36\times10^8$	States	States	$\div 36\times10^5$	$\div 36\times10^5$	$\div 36\times10^2$
1	0	1	1	$\div 6\times10^8$			$\div 6\times10^5$	$\div 6\times10^5$	$\div 6\times10^2$
				—			—	—	—
1	1	1	0	$\div 2\times10^4$			$\div 2\times10^1$	$\div 2\times10^1$	$\div 2\times10^1$
1	1	1	1	Ext. In.	Ext. In.	Ext. In.	Ext. Int.	Ext. Int.	Ext. Int.

*Addresses 1100 and 1101 result in Logic 0 at the output regardless of the state of the Reset Max. and Reset Min. inputs.

Logic 1 = High = V_{SS}
Logic 0 = Low = V_{DD}

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MOSTEK CORPORATION ®

MOS Counter Time-Base Circuit **MK 5009 P** MOSTEK CORPORATION

DESCRIPTION OF OPERATION

The MK 5009 P consists basically of a series of counters, selectable via an internal multiplexer. The ÷ 10^1 counter output is used to generate an internal clock signal for the 10^2 through 36×10^8 counter stages, which are fully synchronous with each other.

OSCILLATOR CONTROLS

Operation in the RC oscillator mode is achieved as shown in Figure 1. Frequency, f, is approximately 0.8/RC. The clamp circuit can be used in the RC mode to provide one-shot or accurate start-up operations. When $\overline{\text{Clamp}}$ goes to a logic 0, the internal circuitry is held at a reference level so that upon release of the $\overline{\text{Clamp}}$ (return to logic 1), the oscillator's first cycle will be a full cycle.

The crystal oscillator mode is shown in Figure 2. Values for the resistors are chosen to bias the internal circuitry for optimum performance. The two capacitors are chosen to provide the loading capacitance (C_L) specified for the selected crystal. It is recommended that C1 = C2 = 2 C_L.

RESET/BYPASS CONTROLS

The MK 5009 P provides two different reset conditions. A positive-going pulse of 10 μs or longer on Reset 0 will reset counters to their lowest state, while a positive-going pulse at Reset Max will reset counters to their highest state. The Reset Max control enables the user to set up the counters to provide a falling edge at the next oscillator cycle or negative-going external input, regardless of which divider chain is selected.

In addition, taking one or both Reset Inputs to the most negative voltage, V_{GG}, allows bypassing portions of the divider chain for testing or other purposes (see table on page 1).

EXTERNAL/INTERNAL FREQUENCY SOURCE

When using an external signal source to operate the MK 5009 P, that signal should be applied at the External Input (Pin 3), and the External/Input Select (Pin 5) should be brought to logic 1.

For operation with an internal signal, the External/Internal Select should be at logic 0.

OSCILLATOR OUTPUT

The oscillator output, provided at Pin 10, is not a true logic output, but may be used to drive a high impedance device such as a junction FET or other MOS circuitry.

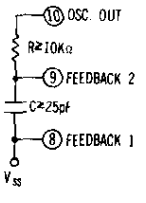


FIG. 1

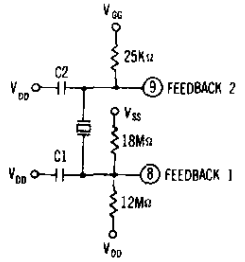
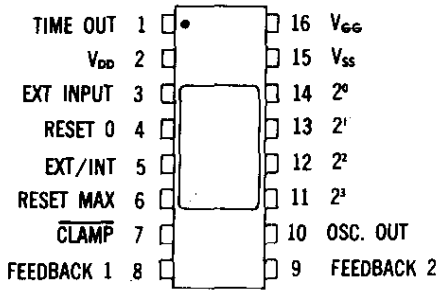
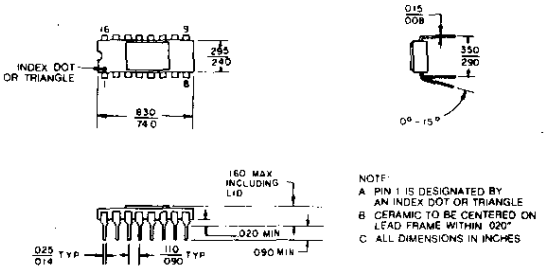


FIG. 2

PIN CONNECTIONS



PACKAGE (16-lead ceramic dual-in-line hermetic package)



NOTE:
A PIN 1 IS DESIGNATED BY AN INDEX DOT OR TRIANGLE
B CERAMIC TO BE CENTERED ON LEAD FRAME WITHIN .020"
C ALL DIMENSIONS IN INCHES

APPENDIX D. CONTROL PROGRAM

Memory Location	Instruction Mnemonic	Instruction Octal	Explanation
70/	$L4_2I$	026 000	Register C = 0
	Lr_0I	006 003	
	OUT4	171 006 000 165 167	Clear I/O Registers
	Lr_5r_0	350 066 376	M = 376
104/	INP0	101	ADC → Accumulator
	OUT2	165	Display ADC
	OUT0	161	Reset & Start ADC
	Lr_1r_0	310	Reg. B = ADC
	INP1	103	A = Hi Alarm
	OUT3	167	Display A
	SUr_1	221	A = (Hi Alarm) - ADC
	JT_{00}	140 131 000	Jmp 131 IF ADC > Hi Alarm
	Lr_0r_1	301 227	A = ADC A = ADC - Lo Alarm
	JT_{00}	104 137 000	Jmp 137 IF Lo Alarm > ADC

	Lr_0I	006 003	Clear Lo & Hi Alarms
	OUT4	171	
	JMP	104 104 000	Jmp 104
131/	Lr I	006 376	Set Hi Alarm
	OUT4	171	
	JMP	104 104 000	Jmp 104
137/	Lr_0I	006 001	
	CPr_2	272	Jmp 151 IF REG.C = J
	JT_{01}	150 151 000	
	INr_2	020	Increment REG. C
	JMP	104 104 000	Jmp 104
151/	Lr_0I	006 375	Set Lo Alarm
	OUT4	171	
	JMP	104 104 000	Jmp 104
376/		040	Lo Alarm = 1/8 full scale[a]

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a. Change data value in Loc. 376 to change low level alarm setting.