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COMPUTER-CONTROLLED IN-LINE MONITORING SYSTEM FOR A RADIONUCLIDES SEPARATION PROCESS

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COMPUTER-CONTROLLED IN-LINE MONITORING SYSTEM FOR A RADIONUCLIDES SEPARATION PROCESS

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ABSTRACT

A dedicated PDP-9 computer was adapted for rapid data acquisition and computation from an in-line Ge(Li) gamma spectroscopy system used to monitor a pressurized ion exchange process for separating and purifying transplutonium elements. Digital discriminating hardware selects for storage only significant portions of a 4096-channel gamma spectrum. Data storage is controlled by the hardware with the direct-access-to-memory feature of the computer. Data acquisition rates are limited only by the processing time of the analog-to-digital converter. Efficient use of hardware significantly simplifies input/output software. Integrated circuit logic modules reduced the cost of the system.

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INTRODUCTION

An in-line system was required for developmental work to collect data from detectors monitoring a chemical process stream containing radionuclides, to compute control parameters from the data, and to supply information and instructions to production operators. Three types of detectors monitor the process stream: a high-resolution Ge(Li) detector produces a gamma spectrum from which specific radionuclides can be identified; a BF_3 neutron detector measures gross neutron activity; and a NaI gamma detector coupled to a single channel pulse-height analyzer measures the high energy gross gamma activity.

To control the process, the system must be capable of acquiring data, computing radionuclide concentrations, and printing out these concentrations every 30 sec. A system configuration was selected that uses a fast analog-to-digital converter (ADC), a special data processing interface, and a dedicated computer. Based on cost, availability, and word length, a Digital Equipment Corporation PDP-9, 8K, 18-bit word computer was selected.

CIRCUIT DESCRIPTION

The computer control system is shown in Figure 1. The only peripheral equipment on the basic PDP-9 computer are a high-speed paper reader/punch, a KSR 35 teletype, and a storage scope display. The only hardware option is an automatic multiply/divide circuit. Outputs for process operators are a typed log sheet, an annunciator panel, and a scope display.

For lower cost and easier maintenance, the DSPI and all control logic interface circuits were built with integrated circuit logic modules, fabricated by point-to-point wire wrapping and housed in modular drawers.

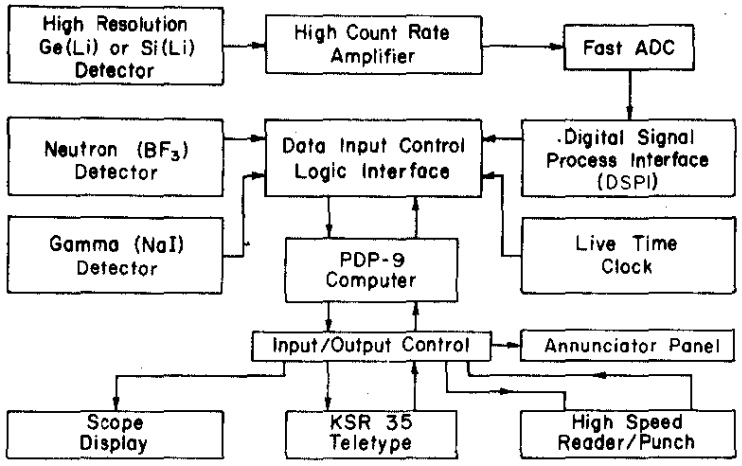


FIGURE 1. Computer Control System

DIGITAL SIGNAL PROCESS INTERFACE (DSPI)

A Digital Signal Process Interface was designed. This interface stores in the PDP-9 computer only data from those channels of the ADC which correspond to significant radionuclides. A 4096-channel ADC was needed because of the energy resolution capabilities of the Ge(Li) detector; however, only ten 50-channel peak regions correspond to significant radionuclides. The spectrum is compressed from 4096 to ∿500 channels by assigning sequential memory addresses to the ten regions. The address for the first data word is selected on the DSPI control panel. The remaining ∿7500 memory locations can be used for operating and computing software.

The ADC output data and the computer control signals are connected to the Digital Signal Process Interface (DSPI) circuit, where the data are compared with upper and lower limits of ten data regions set on thumbwheel switches (Figure 2). Logic signals are described in the Appendix. If the data fall within a selected region, the computer memory address is sent to the PDP-9 computer

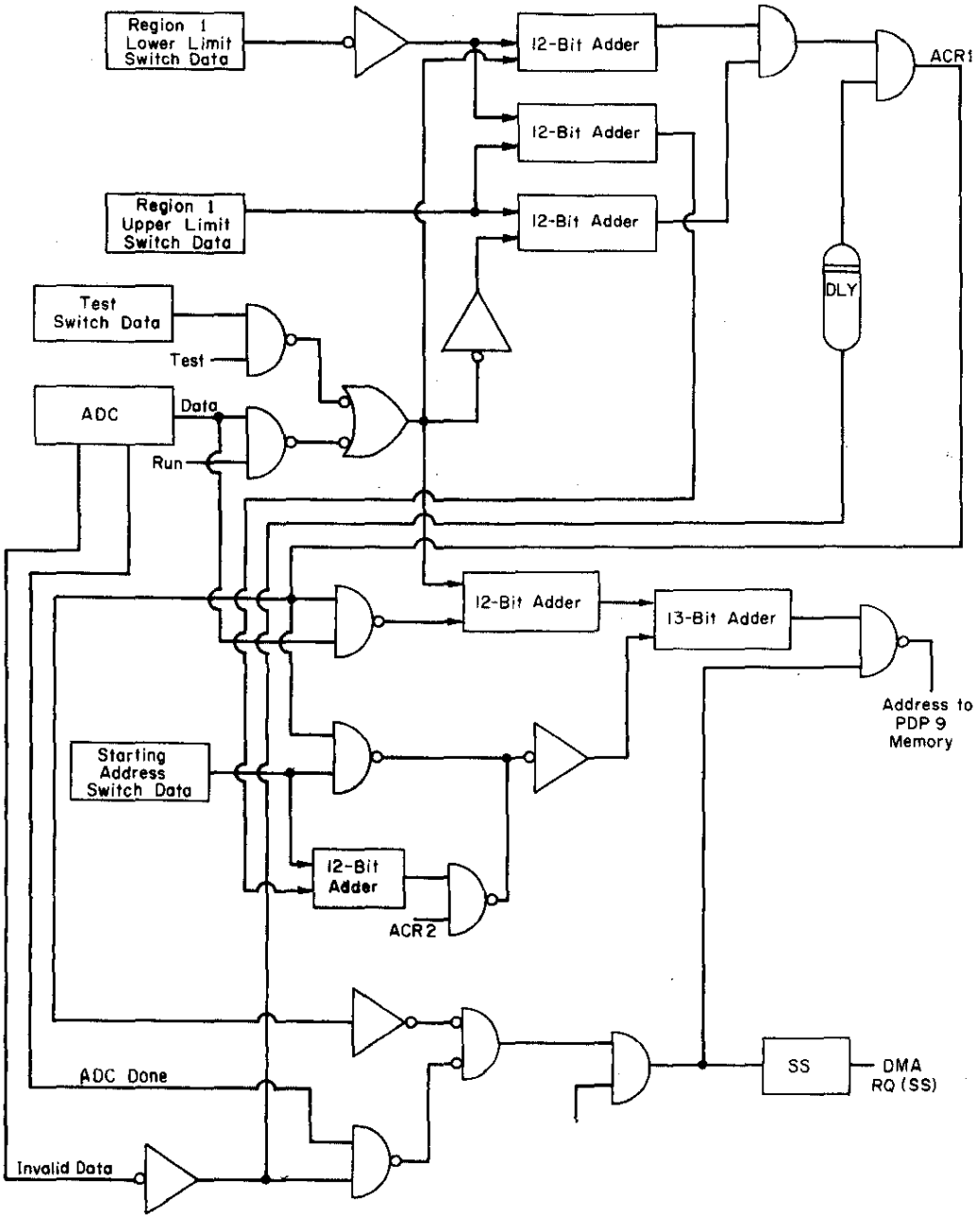


FIGURE 2. Digital Signal Process Interface

memory control logic, and a Direct Memory Access (DMA) request is issued. A program input/output transfer (IOT) command allows ADC data to be processed by DSPI. This command is the only computer control over data acquisition through the DMA channel.

Region limits are set up as octal numbers on four thumbwheel switches. The 12-bit binary limits are connected to ten region discriminators. Any region, or combination of ten regions, may be set up with widths of zero to 7775_8 channels; the sum of the region widths must not exceed 7775_8. Or, the region-selection circuits can be bypassed to store a full 7777_8 spectrum in computer memory. Three 12-bit binary adders in each of the ten digital discriminators do not employ end-around carry arithmetic. Carry signals from the most significant bit adders of the upper and lower limit adders are anded to generate ACRx when data fall between the selected limits. The output of the width adder is the number of channels in the region.

The DSPI ignores ADC data outside a selected region. If the data are within the limits of a region, DSPI signals the PDP-9 computer to execute a DMA cycle at a specified memory address. During the 1-μsec cycle-stealing DMA operation, the computer memory is read into an auxiliary buffer register, incremented by one, and written back into memory. Maximum time for latency and DMA operation is 3 μsec (Figure 3). A circuit modification was made in the PDP-9 memory control logic to allow correct operation of DMA during an IOT or EAE (extended arithmetic element) instruction. Without the modification the DMA will not operate as described in PDP-9 manuals. The minimum time between ADC digitizations is 5 μsec; therefore, the gamma spectrum is acquired and stored at the digitizing rate of the ADC, 5 to 35 μsec per event. If one of the 18-bit data words in memory overflows, a program interrupt signals the computer.

A digital live-time clock is turned on by the computer program. During the counting interval, precision time pulses are counted with an 18-bit binary counter to provide an accurate live time (±1 msec) for computer calculations. When the clock is turned off at the end of a data collection interval, the live time for that interval can be entered into the computer accumulator with a single instruction. Count rates from BF_3 and NaI detectors are in external hardware and stored in memory by program-controlled IOT commands.

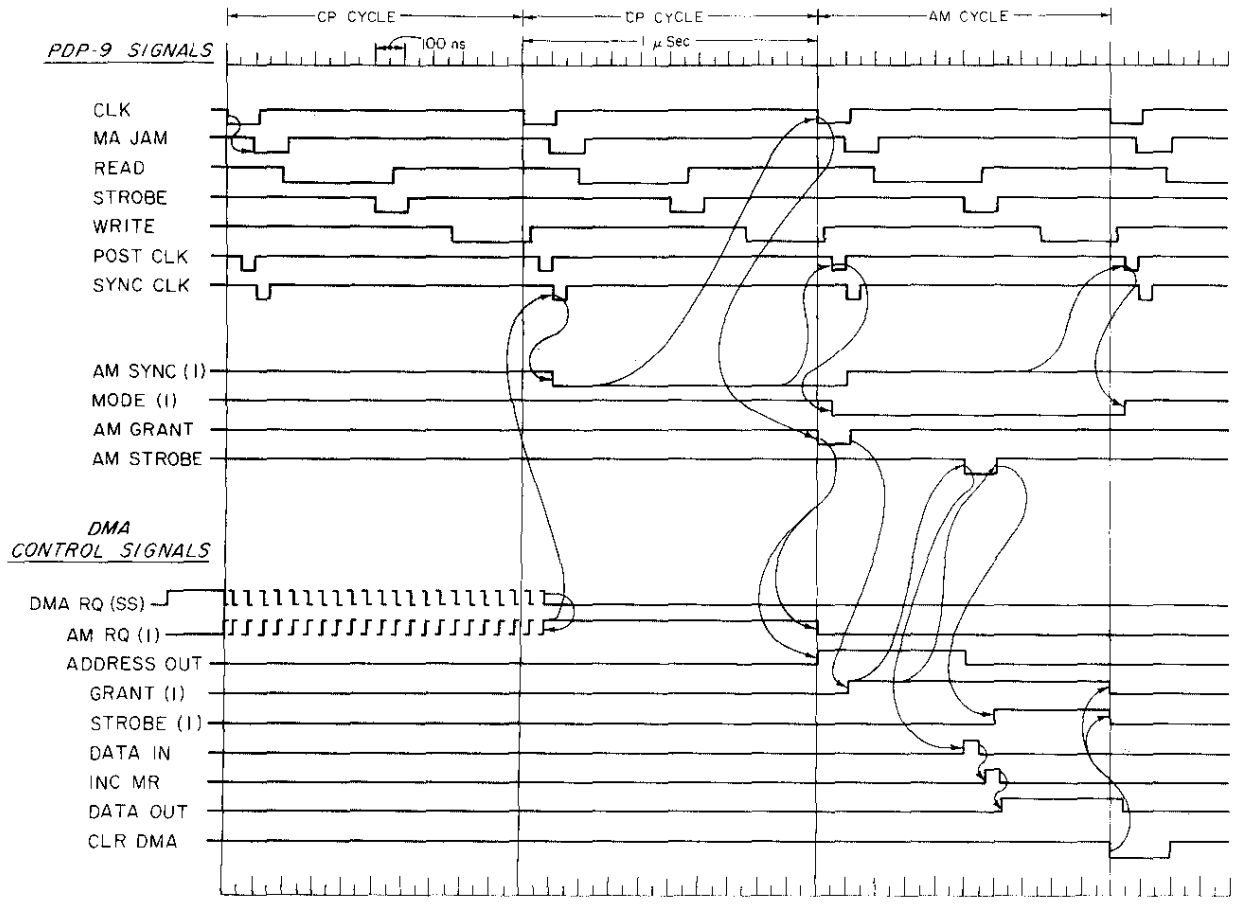
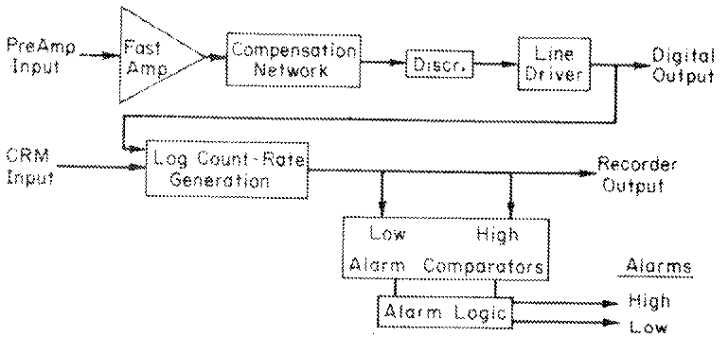


FIGURE 3. Timing Diagram for Direct Memory Access Control

COUNT-RATE CIRCUITS

The BF_3 and NaI detectors are connected to a dual range log ratemeter (Figure 4) for accurate continuous monitoring of count rates. Two 3-decade ranges have a 1-decade overlap. Adjustable high and low alarm outputs, an analog output for current or voltage recorders and a logic output for the computer system are available. The ratemeter incorporates an internal amplifier for low level signals from BF_3 counter preamplifiers. It also accepts an input signal from standard nuclear (NIM) equipment.



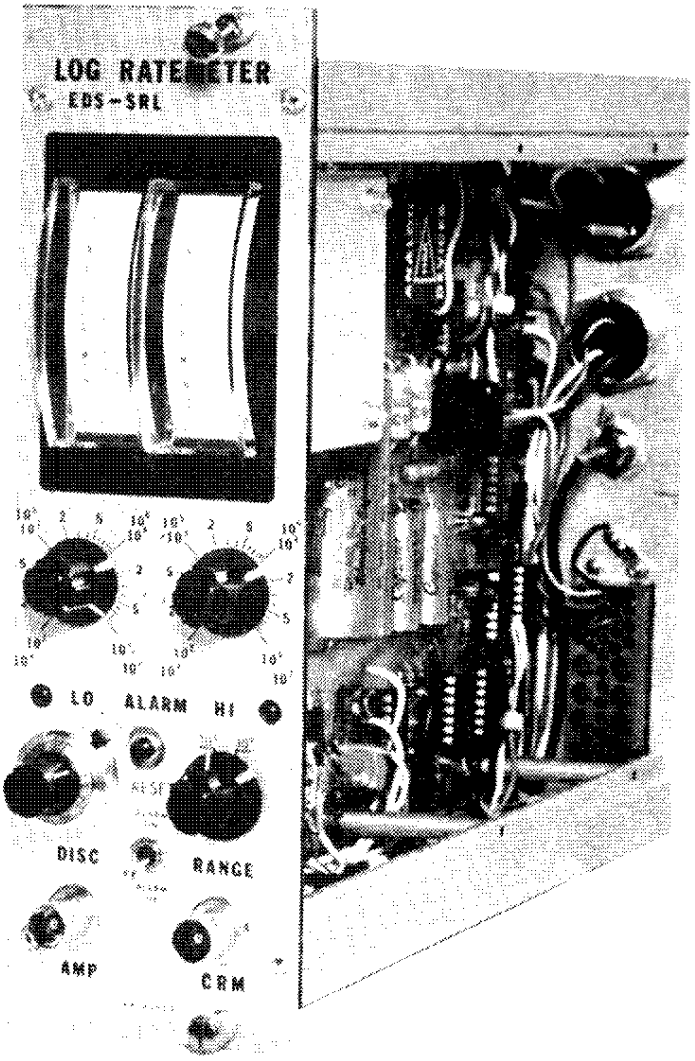


FIGURE 4. Dual-Range Log Ratemeter

Detector pulses are also counted with preset count digital count-rate circuits in the computer interface hardware (Figure 5). Input pulses are counted with an 11-bit synchronous binary counter, C-REG, manually programmed to set a flip-flop, STOP(1), after counting 256, 512, 1024, or 2048 pulses. During that time, 1-msec clock pulses, 1 CLK, are being counted and stored in a binary register, T-REG. At the end of the preset counting interval, time data is transferred to a buffer register, B-REG, for acquisition by the computer with a single IOT command. A timing diagram, Figure 6, shows relative timing for digital signals in Figure 5. The number of counts for a counting interval is selected to give the best statistical accuracy for the count-rate range of input pulses. A future logic revision will allow the computer to select the preset number of counts and to change the number according to conditions set up in the computer program.

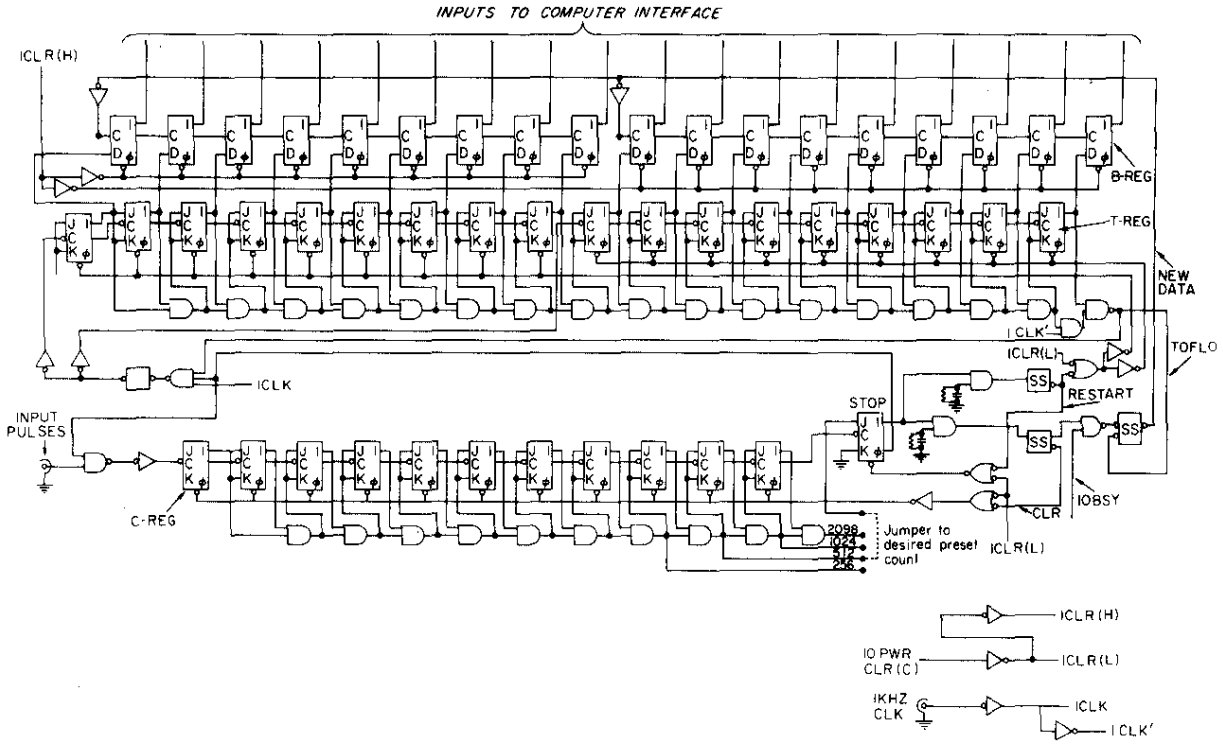
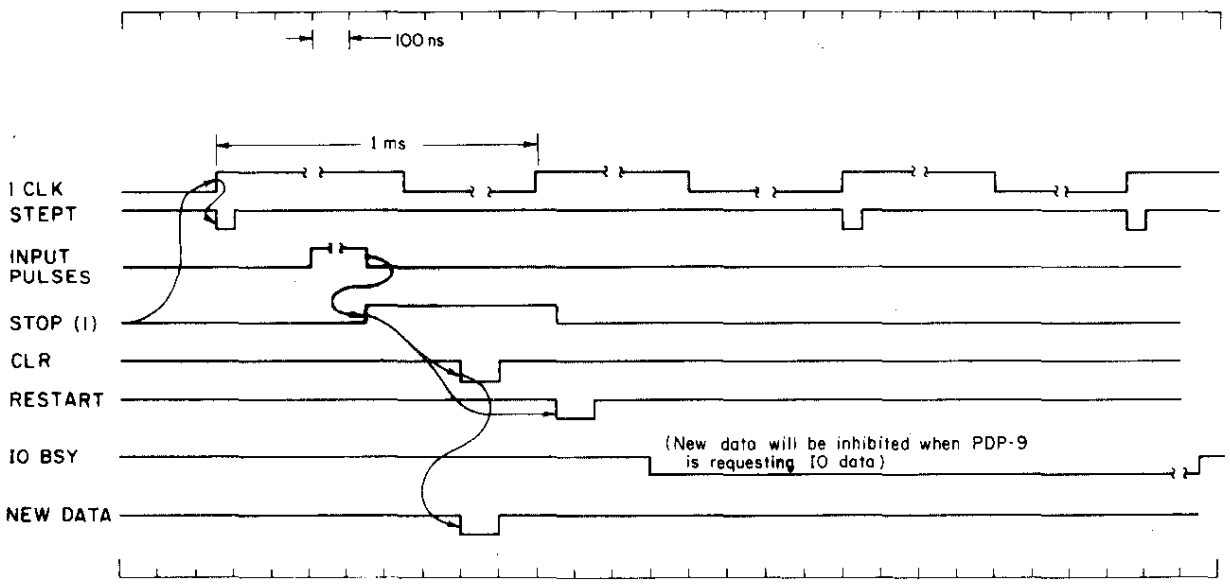


FIGURE 5. Digital Count Rate Circuit



Notes
(1) CLR Resets C-REG
(2) RESTART Resets T-REG
(3) ICLR(L) Resets STOP, C-REG, T-REG, B-REG

FIGURE 6. Count-Rate Timing Diagram

SCOPE DISPLAY

A storage oscilloscope with interfacing provides two display modes, storage and continuous sweep, for flexibility in quick-look data presentation. The interface uses two modular digital-to-analog converters (DAC) for the X-axis and Y-axis display decoding; hardware Y-axis gain selection with five linear or logarithmic ranges is available for operating simplicity (Figure 7).

PERFORMANCE

The computer system described was checked out on a prototype chemical process system. In continuous operation for approximately six months, only a few hours of downtime were required for maintenance. After this maintenance checkout, the system was modified to include a second teletype, additional process inputs for another Ge(Li) detector, and sixteen more count-rate circuits. An annunciator panel and 280 programmed relay contact closures to the process were added (Figure 8).

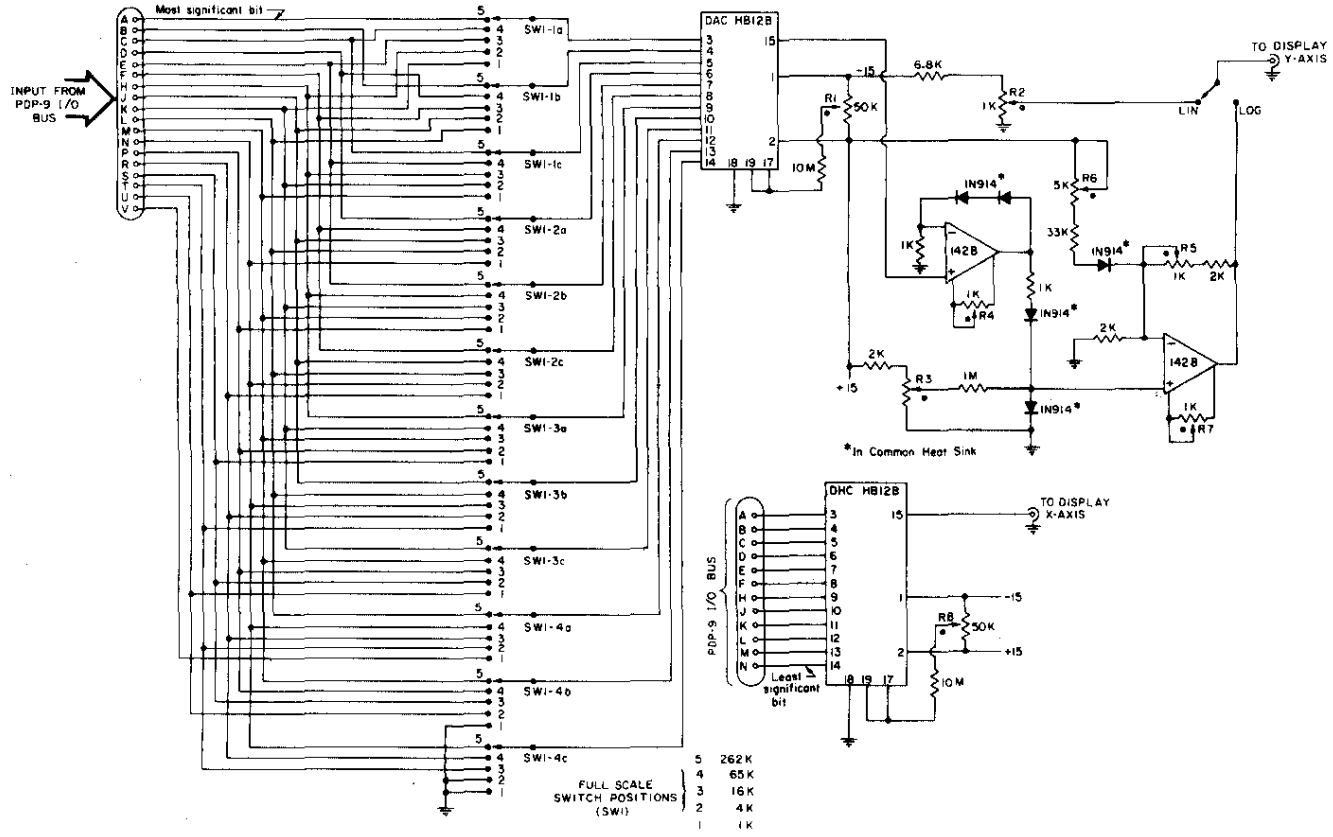


FIGURE 7. Digital-To-Analog Converters for the X- and Y-Axis Display Decoding

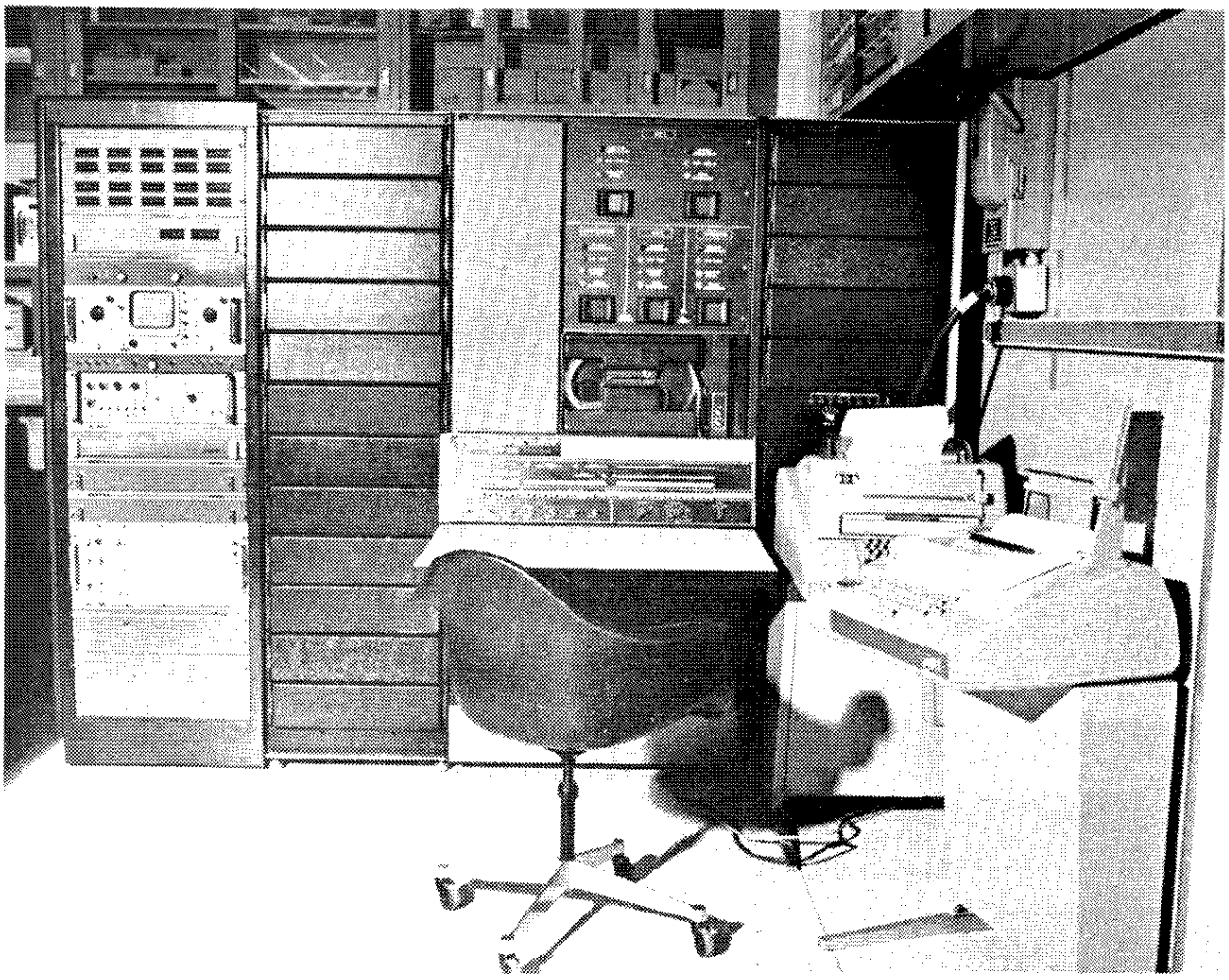


FIGURE 8. Expanded Computer System

The hardware design, using individual IC modules, wire-wrapped in drawers (Figure 9), reduced overall construction costs and facilitated troubleshooting.

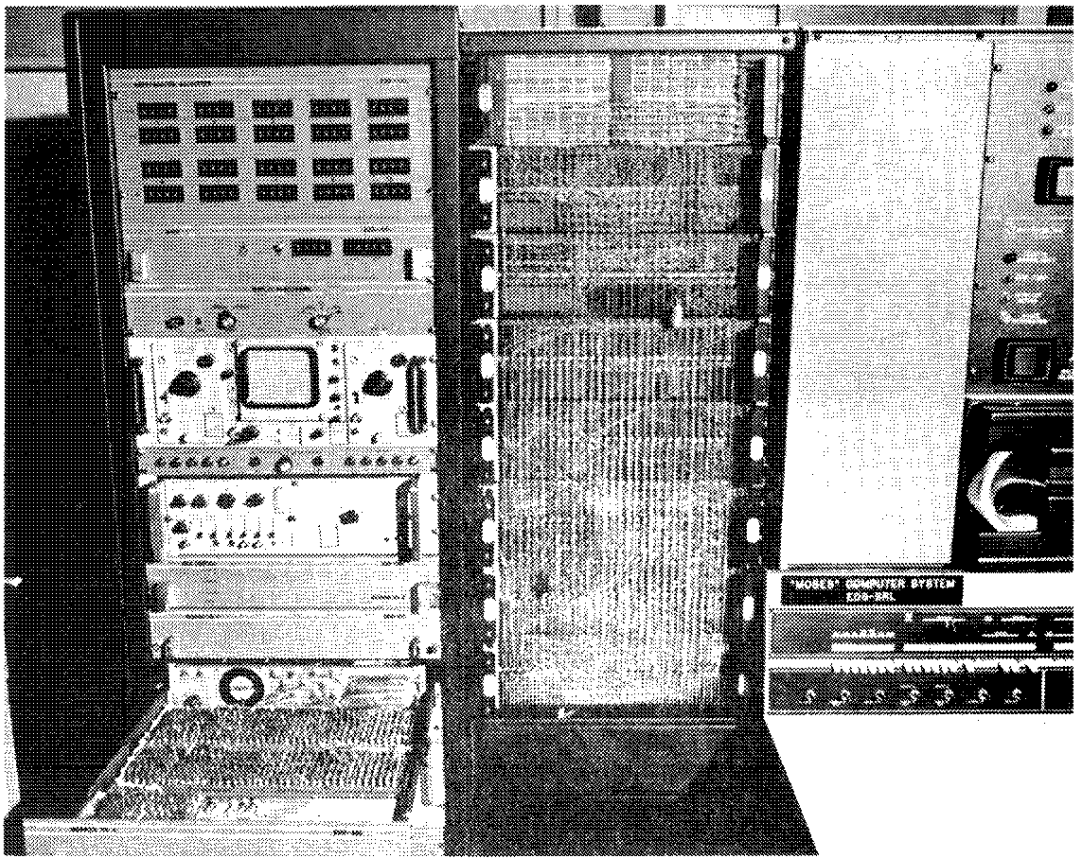


FIGURE 9. Digital Signal Process Interface and Input/Output Wiring to PDP-9

APPENDIX

DIGITAL SIGNALS

Signal	Description
CLK	Pulse clock, 1 per μsec, from PDP-9 computer.
MA JAM	Pulse in PDP-9 to transfer address to memory control logic.
READ	Low level signal during reading portion of PDP-9 memory cycle.
STROBE	Pulse that strobes data to computer memory.
WRITE	Low signal during writing portion of PDP-9 memory cycle.
POST CLK	Delayed clock pulse in computer.
SYNC CLK	Delayed clock pulse in computer.
AM SYNC(1)	Low signal when DMA request signal is acknowledged by computer.
MODE(1)	Low signal in computer during DMA cycle time.
AM GRANT	Pulse from computer to auxiliary device (DSPI) that acknowledges a DMA request.
AM STROBE	Memory strobe signal from computer to DSPI during DMA cycle.
DMA RQ(SS)	High pulse from single shot in DSPI when a DMA cycle address has been set up.
AM RQ(1)	High flip-flop signal from DSPI to PDP-9 to request DMA cycle.
ADDRESS OUT	High signal in DSPI that gates out computer address to PDP-9.
GRANT(1)	High flip-flop output in DSPI when AM GRANT is received by DSPI.
STROBE(1)	High flip-flop output in DSPI after AM STROBE.
DATA IN	High pulse in DSPI that gates memory data from computer to DSPI register during DMA cycle.
INC MR	Pulse to increment contents of DSPI data register.

Appendix (Contd)

Signal	Description
DATA OUT	High pulse that gates incremented data from DSPI back to computer during DMA cycle.
CLR DMA	Clear pulse in DSPI that indicates completion of DMA cycle.
1 CLK	1-KHz precision clock pulse in process interface.
ACRx	Signal to accept data from Region x, when x is 1 to 10.
IO PWR CLR	Reset pulse from PDP-9 computer.
B-REG	18-bit buffer register for count-rate data.
T-REG	18-bit time register for digital count-rate time.
NEW DATA	Single-shot output that gates new data to B-REG.
TOFLO	Overflow signal from T-REG.
IO BSY	Signal from PDP-9 interface during the IOT instruction that transfers data from B-REG to the computer IO bus.
STEP T	Input pulse to T-REG.
RESTART	Pulse that clears STOP flip-flop and T-REG.
STOP(1)	High flip-flop output when preset count is reached.