DP-1212

AEC RESEARCH AND DEVELOPMENT REPORT

IC DIGITAL DATA SYSTEM FOR MÖSSBAUER SPECTROSCOPY

J. S. BYRD

DUPONT
REG. U. S. PAT. OFF.

Savannah River Laboratory

Aiken, South Carolina

LEGAL NOTICE

Printed in the United States of America
Available from
Clearinghouse for Federal Scientific and Technical Information
National Bureau of Standards, U. S. Department of Commerce
Springfield, Virginia 22151
Price: Printed Copy $3.00; Microfiche $0.65

663768

DP-1212

Instruments
(TID-4500, UC-37)

IC DIGITAL DATA SYSTEM FOR MÖSSBAUER SPECTROSCOPY

by

Joseph S. Byrd

Approved by

D. E. Waters, Research Manager
Laboratory Operations and Services Division

January 1970

E. I. DU PONT DE NEMOURS & COMPANY
SAVANNAH RIVER LABORATORY
AIKEN, S. C. 29801

CONTRACT AT(07-2)-1 WITH THE
UNITED STATES ATOMIC ENERGY COMMISSION

ABSTRACT

A fast multichannel scaler with integrated digital control circuits and a 512-word ferrite-core memory was designed to collect and to store data for Mössbauer spectroscopy. System dead time is 2 microseconds. The data spectrum with up to 4.2 billion counts per channel can be displayed on an oscilloscope and punched on computer cards. Variable mode addressing allows forward and backward scanning.

CONTENTS

LIST OF TABLES AND FIGURES

INTRODUCTION

One type of Mössbauer spectrometer generates a triangular velocity waveform that is used in a closed-loop servo system to vibrate a gamma-ray source (alternatively the test specimen) at constant accelerations. Gamma rays passing through the test specimen in a fixed time interval are counted, added to previous data for the same interval, and stored by a multichannel scaler to produce the Mössbauer spectrum of counts versus source velocity. The digital data system is synchronized with a transducer driver operating at constant acceleration. Frequency of driver excitation and the number of storage channels available for data determine the data counting interval. Low dead time between intervals is desirable to minimize loss of pertinent data.

This report describes a fast digital system that operates in conjunction with a transducer driver mechanism[1] and its associated control electronics,[2] designed and fabricated at the Savannah River Laboratory.

SUMMARY

A digital data handling system was designed and fabricated using high speed integrated-circuit (IC) logic modules. The 10-MHz data can be counted with the data scaler. The scaler contents are added to the contents of a memory location, and the sum is stored back into the same memory location in 2 microseconds, the system data dead time. Memory capacity is 4.2 billion counts per channel. The 512-word 32-bit/word memory can contain one 512-channel spectrum or two 256-channel spectra. One of four channel addressing modes is selected to accumulate and display a data spectrum; 256 or 512 channels can be addressed in sequential ascending order or in alternating ascending-descending order. The alternating scans automatically correct for effects due to the varying position of the Mössbauer test source with respect to the nuclear detector.

CIRCUIT DESCRIPTION

Operate and Test Modes (Figure 1)

Four operating modes are available with the OPERATE MODE SWITCH: $DADY_L$, $DISO_L$, REO_L, and $TEST_L$. Logic signals generated in this circuit control the gating for the entire system. The Appendix contains a list of logic signals. A STOP position that holds all circuits in reset condition is provided between active operate modes. The DATA mode allows input pulses to be counted, stored in memory, and displayed on an oscilloscope; this is the normal mode of operation for collecting Mössbauer data. When DISPLAY is selected, input data are disabled. READOUT mode initiates a readout cycle to automatically punch the stored data on computer cards in hexadecimal format. TEST position allows selection of maintenance test conditions with the TEST MODE SWITCH:

1. EVENS - All even-numbered memory channels are incremented by one count during each control cycle.

2. ODDS - Odd-numbered memory channels are incremented.

3. MANUAL - Control cycle can be initiated manually with push-button.

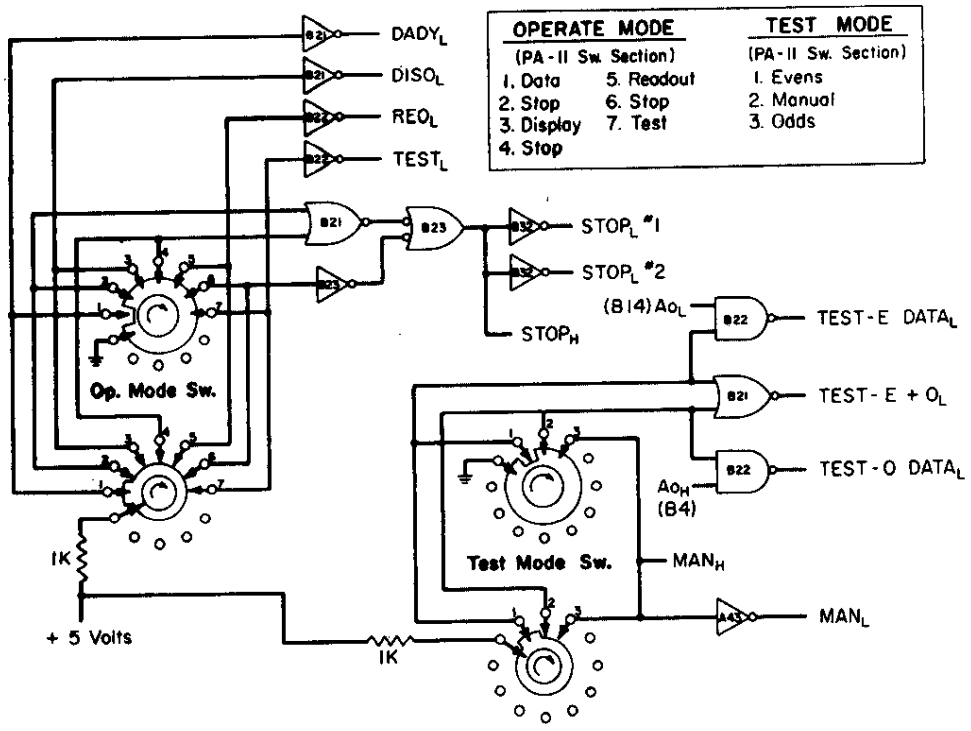


FIG. 1 LOGIC DIAGRAM FOR OPERATE AND TEST MODE SWITCHES

Control Cycle (Figures 2 and 3)

CYCLE CLK_L occurs as shown in the following Boolean expression (see Appendix for terms):

$$\text{CYCLE } CLK_L = (\text{MAN STEP} \cdot MAN_H) + [\text{CAP} \cdot (DADY_L + DISO_L + \text{TEST-E} + O_L)]$$

At the end of the first CYCLE CLK_L, START is set to "1" to enable each subsequent pulse to initiate a read and a write memory cycle, hereafter referred to as a memory cycle. Each CYCLE CLK_L is followed by a data scaling interval. The second CYCLE CLK_L cycles the first channel in the memory unit, channel Ø. At the completion of each memory cycle, CLR DS clears the data scaler, and AAC advances the memory to the next channel. CYCLE CLK_L is 2 microseconds wide and is used as a gating pulse to set the system dead time (Figure 5, A51). REOM and ADV are generated in the punch control circuits.

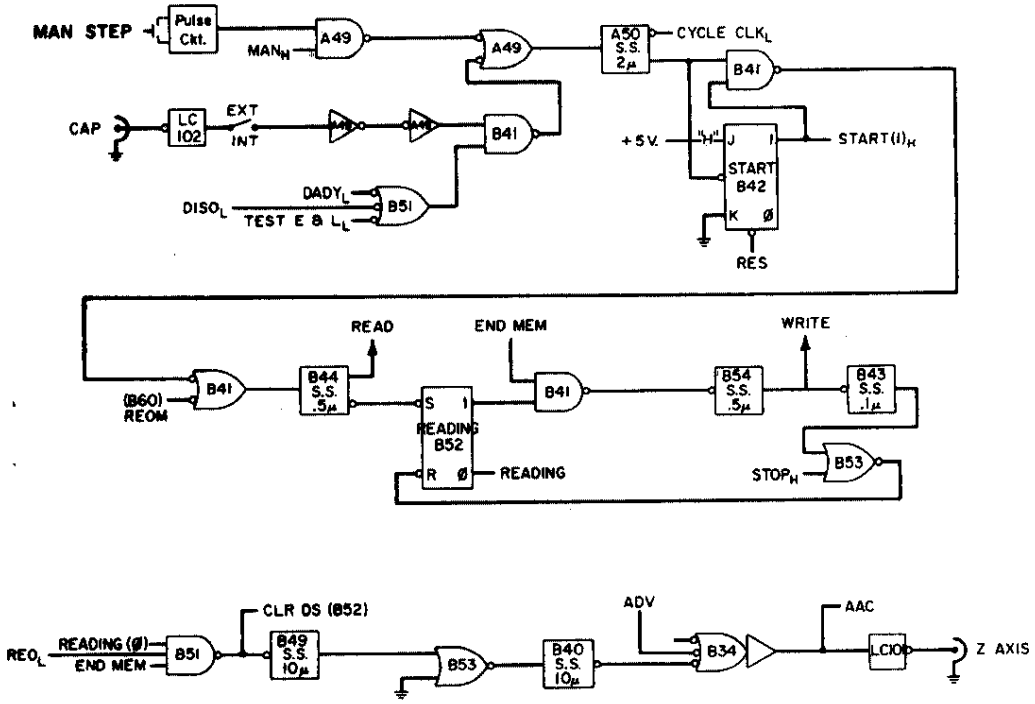


FIG. 2 LOGIC DIAGRAM FOR CYCLE CONTROL

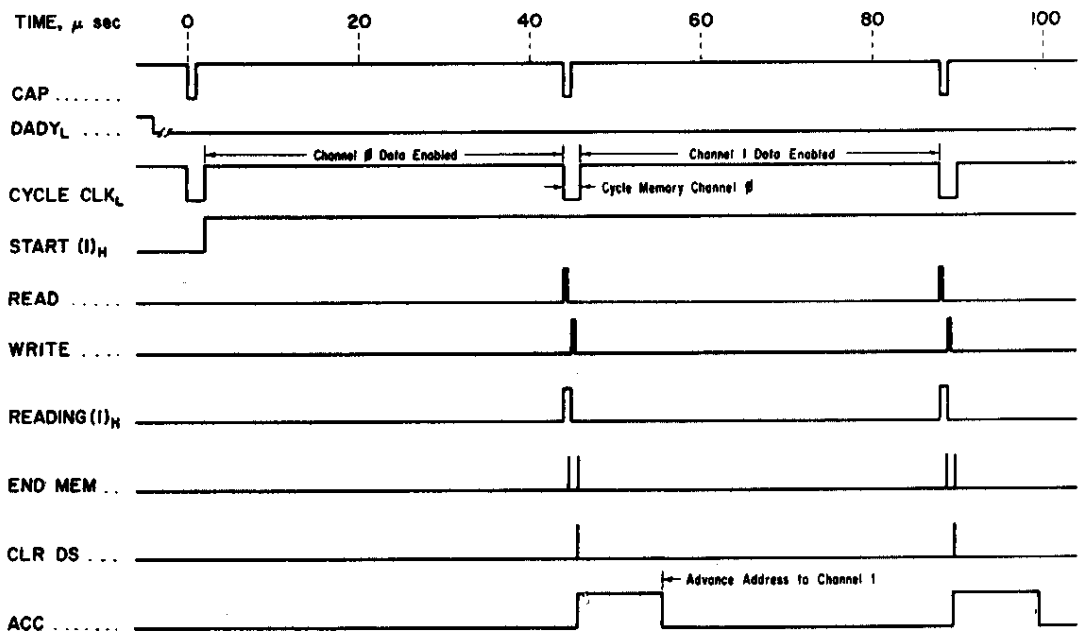


FIG. 3 TIMING DIAGRAM FOR CYCLE CONTROL

Address Counter (Figure 4)

The unique logic for the address counter is given in Reference 3. Four address modes can be selected, as shown in Table I.

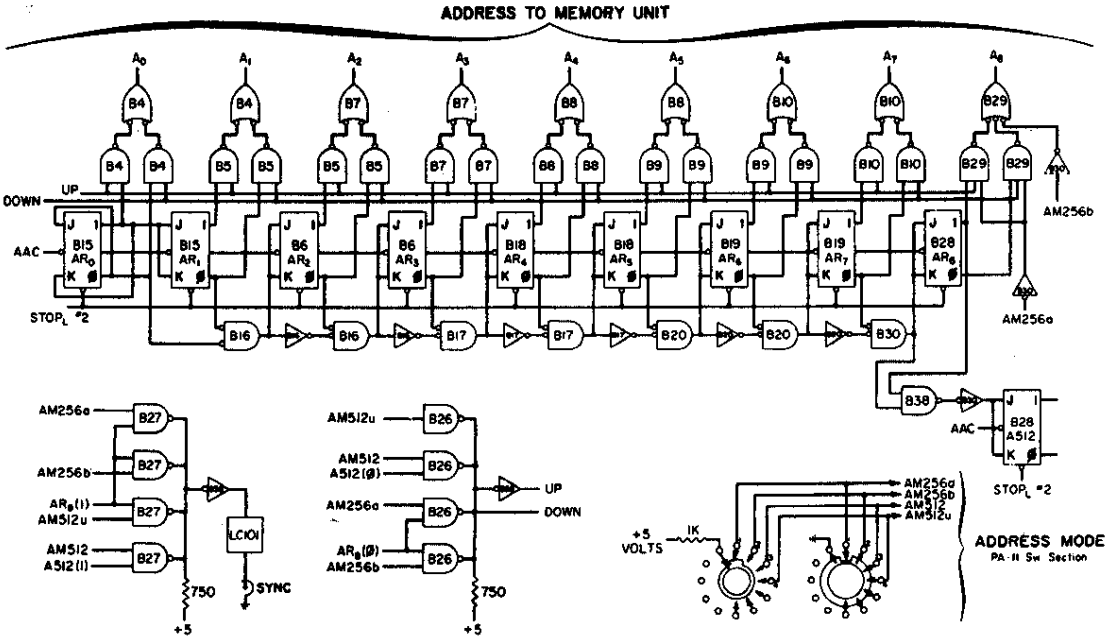


FIG. 4 LOGIC DIAGRAM FOR ADDRESS COUNTER

Table I Address Modes

Mode	Signal Name	Operation
1	AM256a	Scan continuously, in alternately ascending and descending order, memory channels Ø → 255, etc.
2	AM256b	Scan continuously, in alternately ascending and descending order, memory channels 256 → 511, 511 → 256, 256 → 511, etc.
3	AM512	Scan continuously, in alternately ascending and descending order, memory channels Ø → 511, 511 → Ø, Ø → 511, etc.
4	AM512u	Scan continuously, in ascending order only, memory channels Ø → 511

A synchronizing signal, SYNC, is sent to the transducer driver electronics in the Mössbauer spectrometer system. The transducer is driven in one direction when SYNC is a low signal and in the opposite direction when SYNC is high.

$$SYNC_H = AR_8(1) \cdot (AM256a + AM256b + AM512u) + AM512 \cdot A512(1)$$

The effective address outputs, A_0 to A_8, are connected to the memory address inputs and are gated to memory channel selection circuits by the memory unit timing logic.

Data Scaler and Adder (Figure 5)

The capacity of the 10-MHz data scaler, a nine-bit synchronous binary counter, can be increased by adding more flip-flop stages, but this was not necessary due to limitations of the nuclear counter and electronics. Input data are gated with $(DADY_L + MAN_L) \cdot$ CYCLE $CLK_L \cdot$ START $(1)_H$ to advance the scaler.

Nine typical full adder stages are shown in Figure 5. Thirty-two adders, one for each memory data bit, are in the system. One input to all adders is connected directly to the memory output data (DB1-DB32), which are available from the memory register after a memory cycle until the next cycle is initiated. The second input to the least significant nine adders (ADR1-ADR9) is connected to the data scaler (DS1-DS9). The adder outputs (D1-D32) are directly connected to the memory input data gates. During a memory cycle of 2 microseconds, the data are read out from memory, added

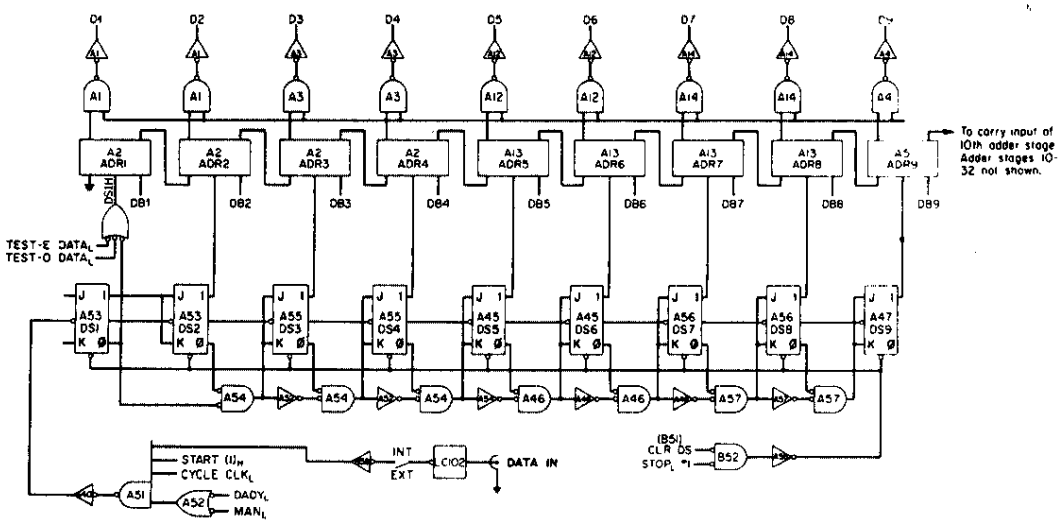


FIG. 5 LOGIC DIAGRAM FOR DATA SCALER AND ADDER

to additional counts from the data scaler, and written back into the same memory location.

The least significant data bit, $DS1_H$, is simulated by TEST-E $DATA_L$ or TEST-O $DATA_L$ during test operations.

Punch Control (Figures 6 and 7)

The punch control logic operates an IBM 026 Card Punch, modified for external digital inputs. Punching rate is established with a 20-Hz free-running oscillator. The oscillator pulses, OSC, are gated to a 5-millisecond single shot (B59).

$$PUNCH\ (1)_H = (DOWN_H + REO_L) \cdot READ\ (\emptyset) \cdot END\ MEM$$

PUNCH (1) through gate B48 drives a Modulo-9 counter (MOD-9) and also establishes the time interval for all punch operations: punch character, space, dash, and release (Figure 7). The MOD-9 provides the nine timing and gating pulses for eight successive hexadecimal data punches (representing 32 binary bits) and a space. A Modulo-8 counter (MOD-8) allows this punch sequence to occur seven times; the eighth time the data punches are followed by a dash punched at column 72 on the card. The card is released and START CARD is set to "1." When a new card is in punch position, START CARD and all flip-flops in the punch control circuit are reset to "Ø" and the punch sequence is restarted. REOM initiates a memory cycle prior to each punch; however, new data from the next channel are set in the memory registers only during a SPACE or DASH, when ADV advances the memory address scaler.

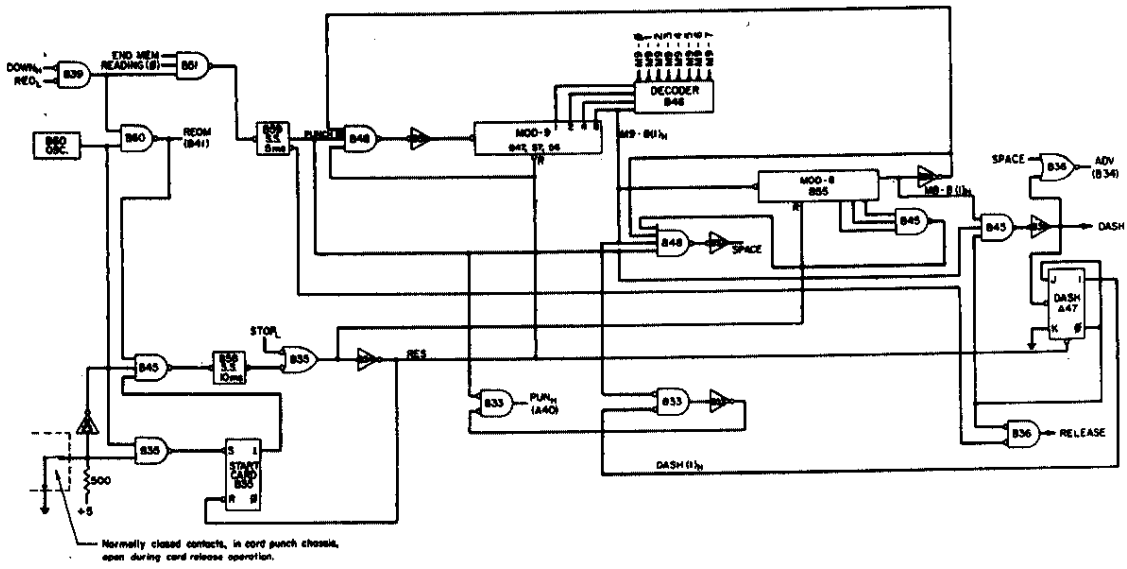


FIG. 6 LOGIC DIAGRAM FOR PUNCH CONTROL CYCLE

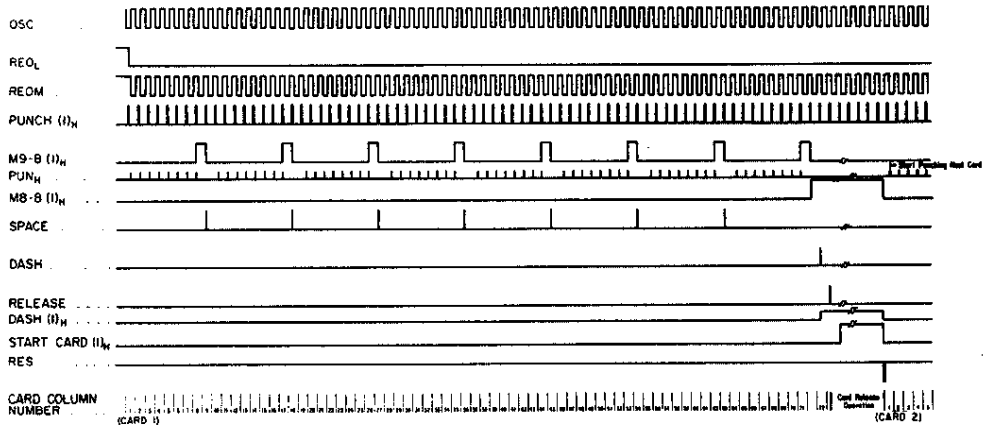


FIG. 7 TIMING DIAGRAM FOR PUNCH CONTROL CYCLE

Punch Decoder (Figure 8)

Thirty-two binary bits read out from memory are decoded to be punched as eight hexadecimal characters with the gates shown on Figure 8. Table II shows the punch input coding.

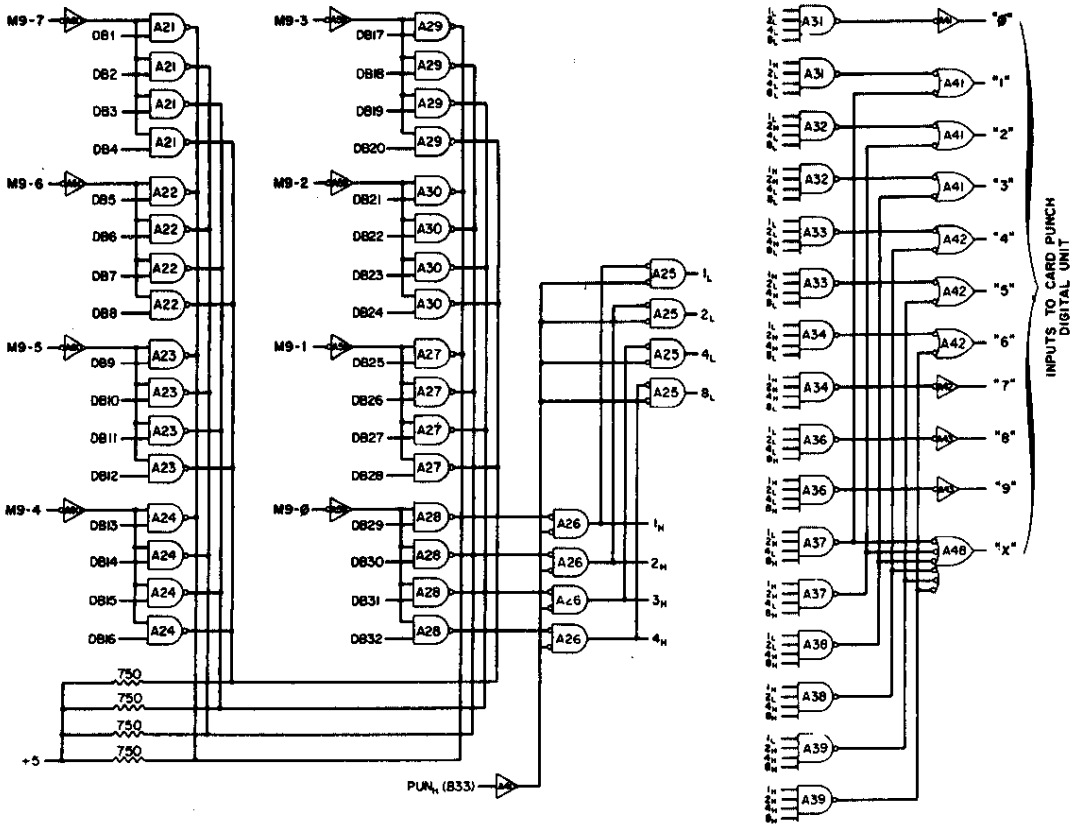


FIG. 8 LOGIC DIAGRAM FOR PUNCH DECODER

Table II Punch Coding

Punch Operation	Signal Required[a]
Punch Ø	"Ø"
Punch 1	"1"
Punch 2	"2"
Punch 3	"3"
Punch 4	"4"
Punch 5	"5"
Punch 6	"6"
Punch 7	"7"
Punch 8	"8"
Punch 9	"9"
Punch A	"x" and "1"
Punch B	"x" and "2"
Punch C	"x" and "3"
Punch D	"x" and "4"
Punch E	"x" and "5"
Punch F	"x" and "6"
Release Card	RELEASE
Punch a Dash	DASH
Space	SPACE

[a] See Figures 6 and 8.

Scope Display Circuits (Figure 9)

Two digital-to-analog converters (DAC) generate 0- to 10-volt signals to drive the X- and Y-axis of an oscilloscope for data display. The X-axis DAC decodes the nine adder bits, A_0-A_8, from the addressing logic (Figure 4) for a horizontal sweep. The vertical display dots, formed by modulating the scope Z-axis, are positioned by decoding the eight data bits from the memory data output signals, DB1-DB32. An 8-pole, 24-position rotary switch selects the vertical sensitivity by routing the eight least significant data bits to the DAC in the first position and the eight most significant bits in the last position. The display dot is 10 microseconds wide, set by AAC (Figure 2).

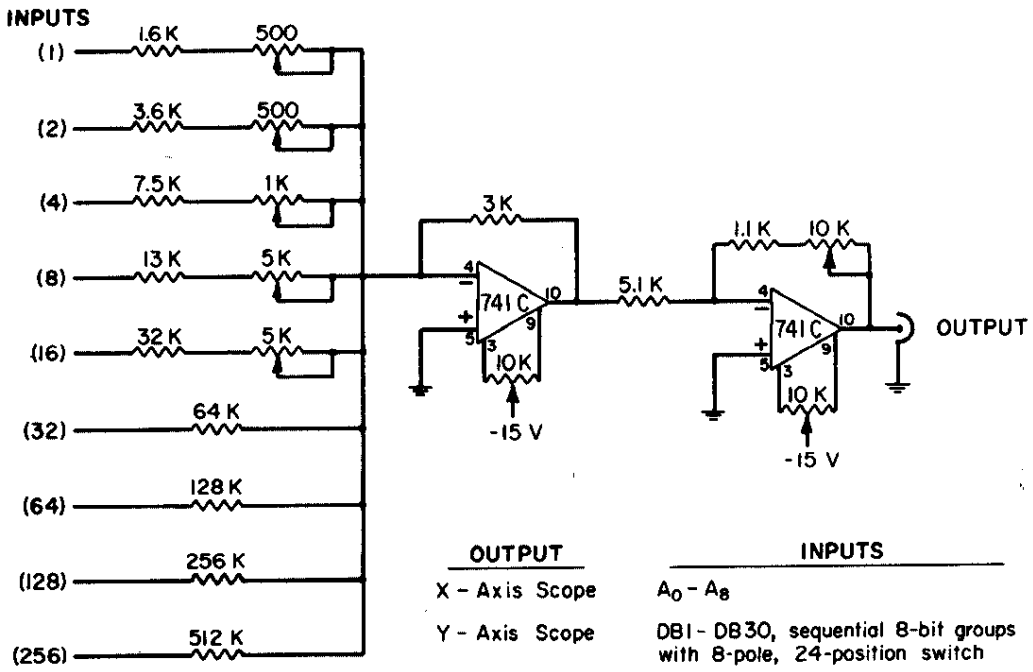
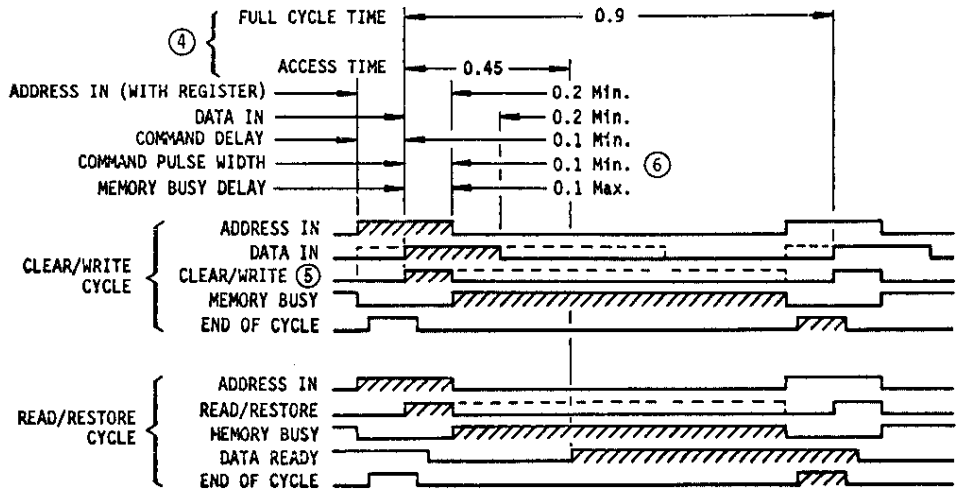


FIG. 9 CIRCUIT DIAGRAM FOR DIGITAL-TO-ANALOG CONVERTER

Memory Unit (Figure 10)

The memory unit is a Datacraft* Model DC-30 with 512 words, 32 bits/word, 1 microsecond full cycle time, and random access. This unit was selected on basis of cost, speed, and compatible internal logic.



NOTES:
1. POSITIVE LEVEL IS TRUE.
2. ALL SIGNALS ARE SHOWN AT MAX. RATE.
3. ALL TIMES IN MICROSECONDS.
4. TIMES SHOWN ARE TYPICAL OF SMALL MEMORIES AND MAY INCREASE FOR LARGE MEMORIES.
5. DATA MUST BE APPLIED WITHIN 0.32 MICROSECONDS AFTER CLEAR/WRITE COMMAND. DATA CAN BE APPLIED UP TO 0.1 MICROSECOND PRIOR TO CLEAR/WRITE COMMAND. UNLESS OTHERWISE SPECIFIED, IT IS ASSUMED DATA WILL REMAIN STABLE FOR THE FIRST 0.2 MICROSECONDS FOLLOWING RECEIPT OF THE CLEAR/WRITE COMMAND.
6. MAXIMUM COMMAND PULSE WIDTH FOR FULL CYCLE OPERATION IS 0.8 MICROSECOND. MAXIMUM COMMAND PULSE WIDTH FOR SPLIT CYCLE OPERATION IS 0.4 MICROSECOND.

FIG. 10 TIMING DIAGRAM FOR MEMORY UNIT

* Datacraft Corporation, Fort Lauderdale, Florida.

Electronic Fabrication (Figures 11 and 12)

Individual TTL IC modules, 7400N series, are plugged into two 60-module socket panels with common voltage and ground planes (Figure 11). Point-to-point wire-wrapping is used to realize the logic design (Figure 12). The logic is powered by a 5-volt, 5-ampere supply. A 12-volt, 1-ampere supply drives incandescent indicator lamps, logic level converters, and relay drivers for the card punch.

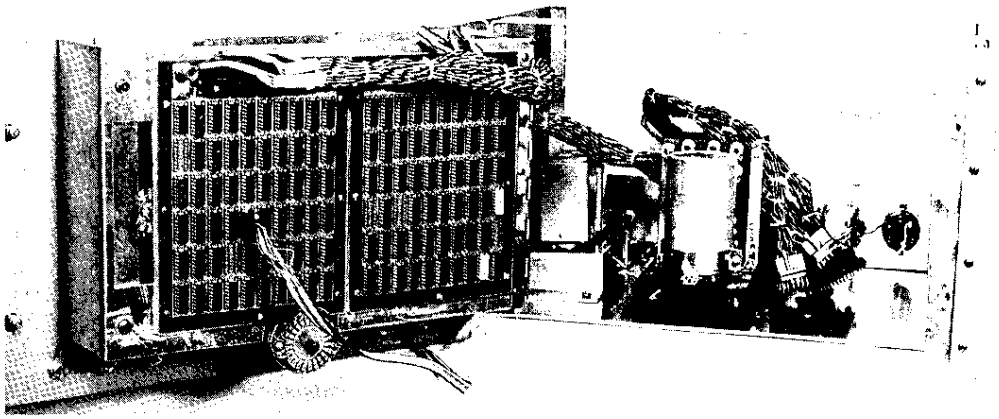


FIG. 11 IC MODULE LAYOUT

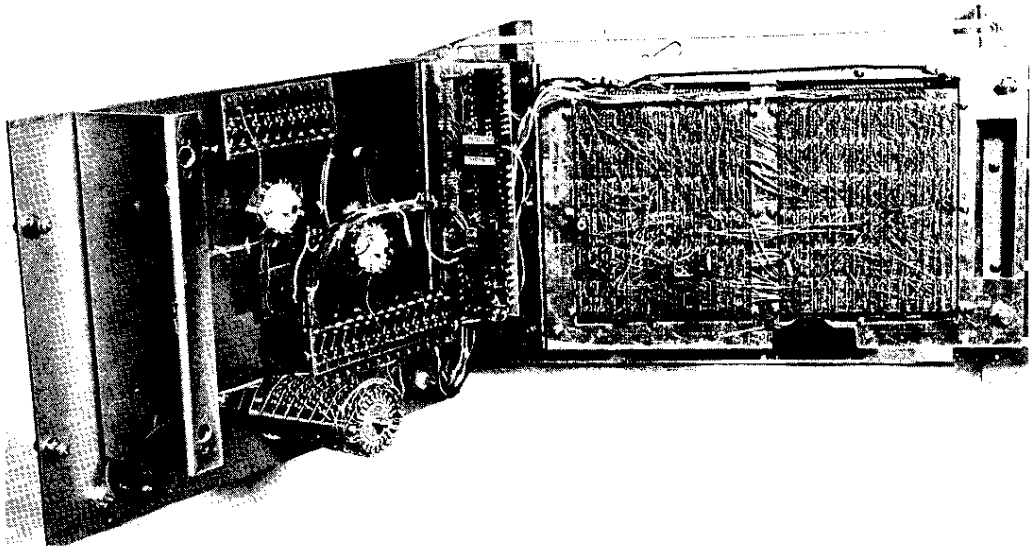


FIG. 12 WIRE-WRAPPED TERMINALS

Mechanical Fabrication (Figures 13 and 14)

A double-hinged door assembly provides easy access to the IC modules and the wiring for ease in maintenance. The control unit is mounted on a rack, 10-3/4 x 19 inches (Figure 13). The memory unit is 5-1/4 x 19 inches (Figure 14).

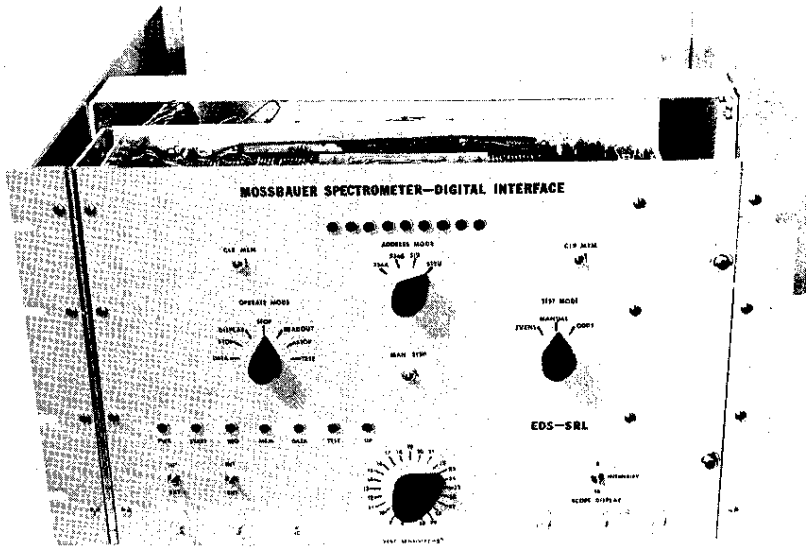


FIG. 13 FRONT VIEW OF CONTROL UNIT

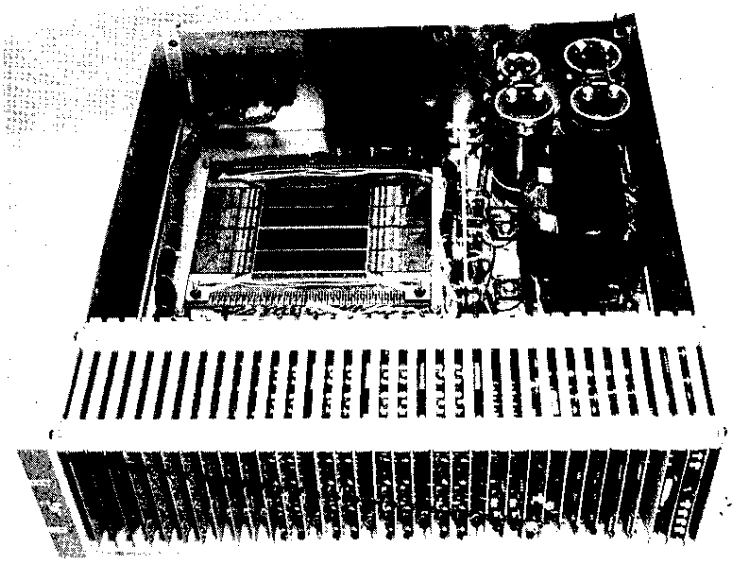


FIG. 14 DC-30 MEMORY UNIT

PERFORMANCE

The system has operated 24 hours a day trouble-free for the past six months with no component failures.

ACKNOWLEDGMENT

The author acknowledges with appreciation the excellent work of J. D. Jenkins for the electronic and mechanical fabrication of this system.

APPENDIX - DIGITAL SIGNALS AND TERMS

Signal or Term	Description
$DADY_L$	Activated by OPERATE MODE Sw. Collect and display data.
$DISO_L$	Activated by OPERATE MODE Sw. Display data only.
REO_L	Activated by OPERATE MODE Sw. Initiates readout cycle, data in memory punched on cards.
$TEST_L$	Activated by OPERATE MODE Sw. Allows test mode to be selected by TEST MODE SW.
STOP #1, #2, $STOP_H$	Stop signal from OPERATE MODE Sw. Holds all registers and operations in stop condition.
TEST-E $DATA_L$	TEST MODE signal. Simulates $DS1_H$ for all even-numbered memory channels.
TEST-O $DATA_L$	TEST MODE signal. Simulates $DS1_H$ for all odd-numbered memory channels.
TEST-E + O_L	Low active level for TEST EVENS or TEST ODDS operation.
MAN_H	Active level for MANUAL TEST.
CAP	Channel Advance Pulse, input timing pulse from transducer electronics circuitry. Fundamental timing clock.
CYCLE CLK_L	2-μs pulse from single shot (A50). Controls memory cycle and input data gating. Determines 2-μs system dead time.
START	Control flip-flop (B42). Starts memory cycles after first CYCLE CLK.
READ	500-ns pulse to memory unit to initiate full-cycle read operation.
WRITE	500-ns pulse to memory unit to initiate full-cycle write operation.

Signal or Term	Description
READING	Flip-flop (B52), active "1" state during memory operation.
END MEM	Pulse from memory after a read or write operation.
CLR DS	Clears data scaler to "Ø" state.
ADV	Initiates an advance address counter pulse during data punching operation.
AAC	Signal to advance address counter, one address.
Z-AXIS	Dot display pulse to oscilloscope.
$REOM_L$	Initiates memory cycle during data punching operation.
RES	Reset pulse generated by STOP or after a card release during punching.
AM256a	ADDRESS MODE, Sw. position 1.
AM256b	ADDRESS MODE, Sw. position 2.
AM512	ADDRESS MODE, Sw. position 3.
AM512u	ADDRESS MODE, Sw. position 4.
AR_0-AR_8	Address counter flip-flops.
A_0-A_8	Address data to memory unit. A_0 is least significant bit.
A512	Control flip-flop and address circuitry.
UP	Active high signal when addresses are scanned in ascending order.
DOWN	Active high signal when addresses are scanned in descending order.
SYNC	Output synchronizing signal to transducer electronics control of Mössbauer spectrometer system.
DATA	Input data from Mössbauer counter electronics.

Signal or Term	Description
D1-D32	Data to memory unit. D1 for least significant bit.
ADR1-ADR32	Thirty-two full adders, one for each data bit to memory unit.
DS1-DS9	Data scaler flip-flops. Accumulates data counts during counting portion of cycles. Counting time set by CYCLE CLK_L.
$DS1_H$	Least significant data, real or simulated, from data scaler to adder.
DB1-DB32	Data from memory unit buffer register.
OSC	20-Hz free-running oscillator for punch cycle timing.
PUNCH(1)	High active output from 5-ms single shot.
PUN_H	5-ms pulse to establish time to close relays for card punch operation.
MOD-9	Four flip-flops connected as Modulo-9 counter.
DECODER	BCD to decimal decoder circuits.
MOD-8	Four flip-flops connected as Modulo-8 counter.
START CARD	Control flip-flop for card release operation. Synchronizes release operation with readout oscillator, OSC.
SPACE	5-ms pulse, initiates a card space.
DASH	5-ms pulse, initiates a dash to be punched.
RELEASE	5-ms pulse, initiates a card release.
MAN STEP	Mechanical pushbutton to initiate a control cycle.

REFERENCES

1. W. L. Pillinger and J. A. Stone. *Mössbauer Effect in Ferredoxin.* USAEC Report DP-878, E. I. du Pont de Nemours & Co., Savannah River Laboratory, Aiken, S. C. (1964).

2. M. H. Goosey. E. I. du Pont de Nemours & Co., Savannah River Laboratory, Aiken, S. C. (unpublished data).

3. J. S. Byrd. "Variable-Mode Counting with Straight Binary Counters." *IEEE Transactions on Computers* (submitted for publication).