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AEC RESEARCH AND DEVELOPMENT REPORT

DIGITAL SYSTEM FOR FAST PRINTOUT OF ANALYZER MEMORY

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Instruments
(TID 4500)

DIGITAL SYSTEM FOR FAST PRINTOUT OF ANALYZER MEMORY

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ABSTRACT

A digital control circuit and code converter was designed to print out the binary data stored in a 4,096-channel spectrum analyzer memory. Data and channel identification are printed in decimal form with a high speed digital printer. The entire memory or any multiple of 256-channel subgroups can be printed parallel at the rate of 40 lines per second.

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DIGITAL SYSTEM FOR FAST PRINTOUT OF ANALYZER MEMORY

INTRODUCTION

The Nuclear Data Model 160 Pulse Spectrum Analyzer stores data in a 4,096-channel, 18-bit, binary core memory. The data can be displayed on an oscilloscope for a "quick look" at the pulse spectrum, or the data can be transferred to magnetic tape in IBM format. However, no provision was made for a fast printout of data for an accurate "quick look" point-by-point analysis of the stored spectrum.

This report describes a digital control circuit with binary-to-BCD (binary coded decimal) code conversion logic to provide fast data printout.

SUMMARY

A digital logic control circuit and code converter was designed and fabricated to print out the binary data from the 18-bit, 4,096-channel memory of the Nuclear Data Model 160 Spectrum Analyzer with a Franklin 1200 High Speed Printer. Memory data and channel identification are printed in decimal form with the 12-column, parallel printer at a rate of 40 lines per second. The 4,096 channels, or words, are subdivided into groups of 256; any selected number of subgroups may be printed.

The circuit was built with modular plug-in logic cards. The particular type selected on the basis of cost, speed, and reliability for this application were integrated circuit (IC) transistor-transistor-logic (TTL) modules. A total of 52 cards of 14 different types and an automatic wire-wrap fabrication technique were used.

Although this circuit was for a particular application with the ND-160 Analyzer and the Franklin 1200 Printer, it could be easily modified for use with similar equipment.

CIRCUIT DESCRIPTION

Cycle Control (Figure 1)

The digital control circuit was designed around a 500-kilohertz clock. The frequency selected for the clock was determined by the type logic modules used – fast enough for the shifting operation time to be negligible compared to the overall print cycle time (approximately 25 ms). Figure 2 shows the timing diagram. A print or scan cycle is initiated by depressing the "Start" push-button. An "Ext IRC" signal (see Appendix for description of all signals) is generated; this signal starts the memory readout cycle in the ND-160, sets up its memory register with the contents of the first channel, and advances its channel scaler to the next address. After a "Start Delay" the cycle clock is enabled for 19 pulses and then disabled by the "MOD 18" counter. The first clock pulse "Data Enable CLK" enables the data gates of an 18-bit shift register; the ND-160 memory register is gated into the 18-bit shift register at that time. The next 18 clocks, "Shift CLK", serially shift the 18-bit data word out of the shift register into the binary-to-BCD converters. The "MOD 18" counter will send a "Print Command" signal to the Franklin 1200, if the "Print" flip-flop has been conditioned to print. After the Franklin has printed a line, the cycle is repeated, and the "Address Buffer/Counter" is stepped with "Step AB."

Print Control (Figure 3)

The circuit will generate "Print Command" and print a line only when the "Print" flip-flop is set for the true output of "Print(1)." If "Print(Ø)" is true, the control cycle will scan through without printing the data. During this scan, the analyzer memory is also scanned. By controlling the inputs to the "Print" flip-flop, any number of the 256-work subgroups can be selected to be printed. A binary-numbered toggle switch selection circuit for "Start Print Address" and "Stop Print Address" was used to minimize the logic modules in this portion of the circuit. The "MOD 17" is stepped every 256 words with a signal from the ND-160. This eliminated the need for decoding the BCD address registers in this system.

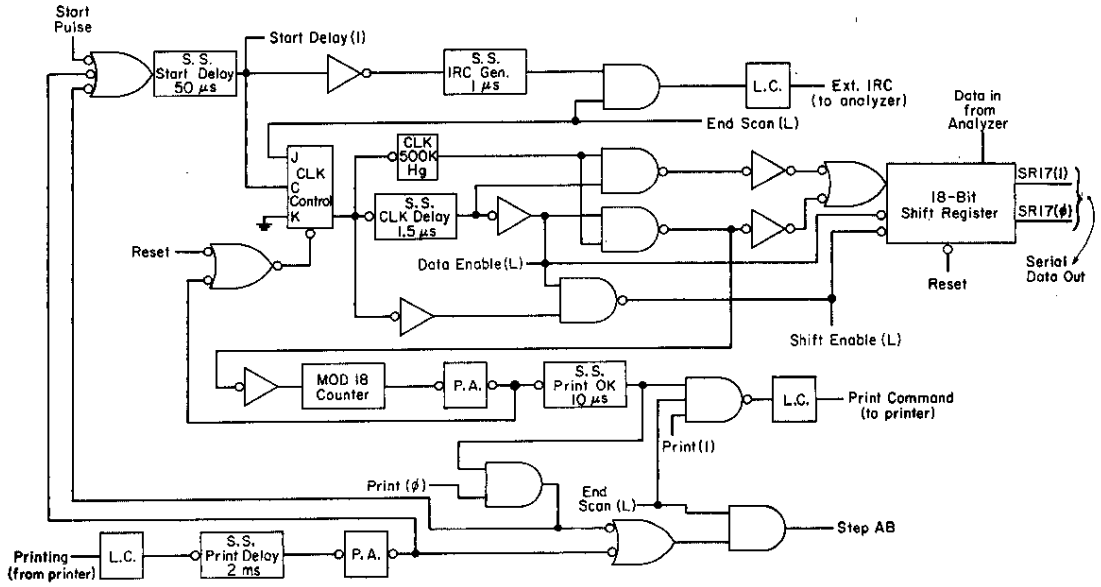

FIG. 1 CYCLE CONTROL
(Simplified Diagram)

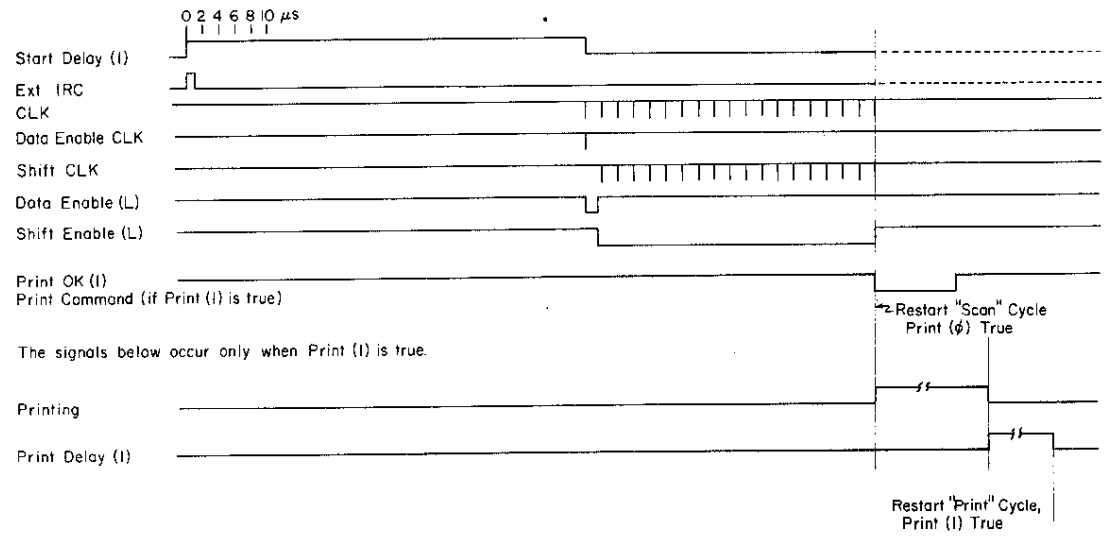

FIG. 2 TIMING DIAGRAM

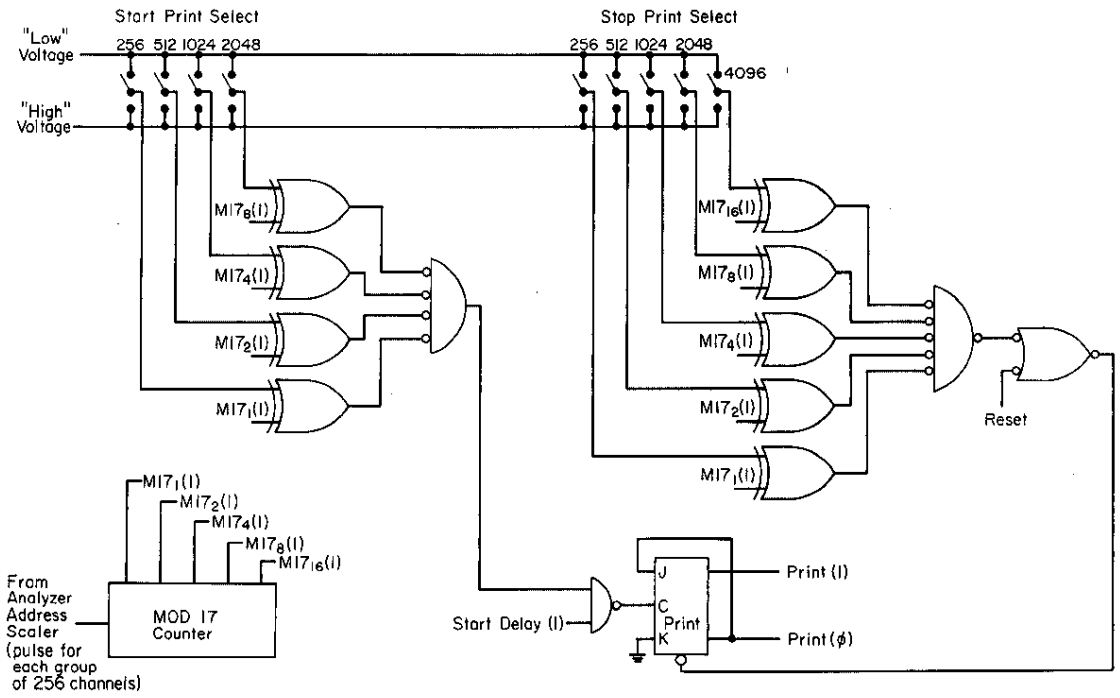

FIG. 3 PRINT CONTROL
(Simplified Diagram)

Address Counter/Buffer

The channel address is printed with the data on each printed line. The binary address information was available in the ND-160 address scaler; however, this binary address would have to be converted to BCD before it could be used as an input to the Franklin 1200 Printer. Therefore, four decade counters were used to count the print control cycles; the BCD address data is then available for printing. The last memory word, channel 4,095, is decoded to end the control cycle and reset all registers.

BCD Converters (Figure 4)

The binary-to-BCD conversion[1] is accomplished using gated shift register stages; the most significant binary digit from the 18-bit shift register, "SR17", is shifted into the least significant BCD digit of the converter. A "carry" is generated to the

1. H. J. Ganes. "Speed Up Binary-to-Decimal Conversion." *Electronic Design* 15 (20), 50 (1967).

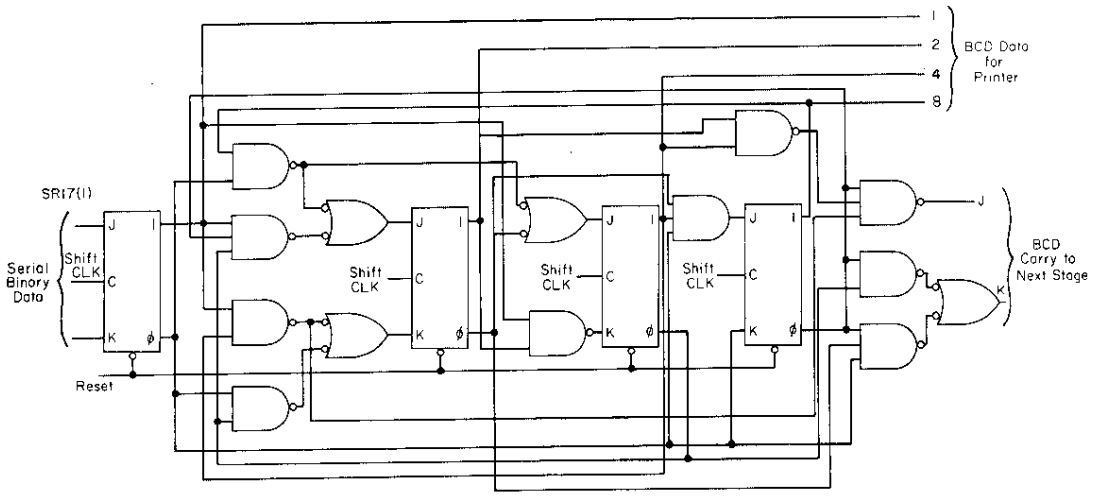

FIG. 4 BCD CONVERTER STAGE
(Simplified Diagram)

next most significant converter stage when the binary number shifted in exceeds decimal nine. Six BCD converter stages are cascaded to decode the maximum 18-bit binary word, which is 242,143 decimal. The 18-digit binary word converts to a 6-digit BCD word in the time required for 18 clock pulses.

Mechanical Design and Fabrication

The logic circuits were built in a chassis 19 inches wide, 7 inches high, and 14 inches deep; front and rear panels were hinged for easy maintenance access (Figure 5). Point-to-point wire-wrapping wiring technique was used. Several indicator lamps were installed to aid maintenance.

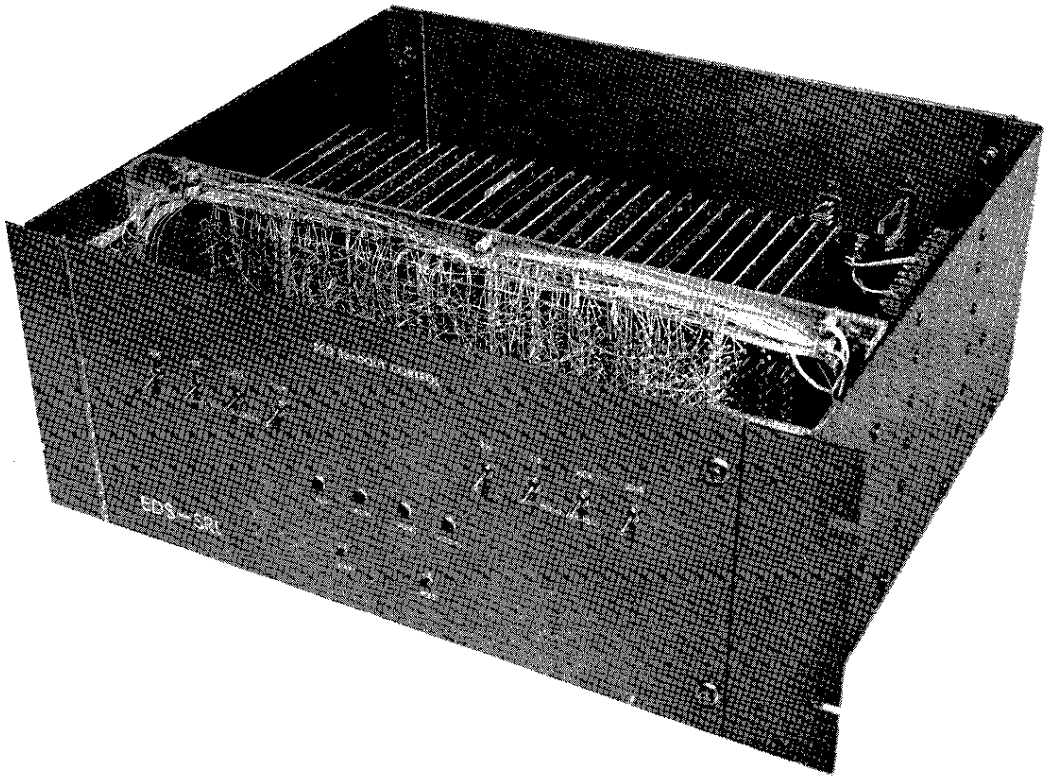

FIG. 5 INSTRUMENT CHASSIS

PERFORMANCE

The digital system (Figure 6) was connected to the analyzer and has performed satisfactorily, providing accurate quick look results. The scope presentation on the analyzer is used to determine the memory address of the particular areas of interest in the stored spectrum (peaks, for example).

Several components in the commercial logic modules failed during the first two weeks of operation, but these are thought to be burn-in failures because no components failed during the following three months.

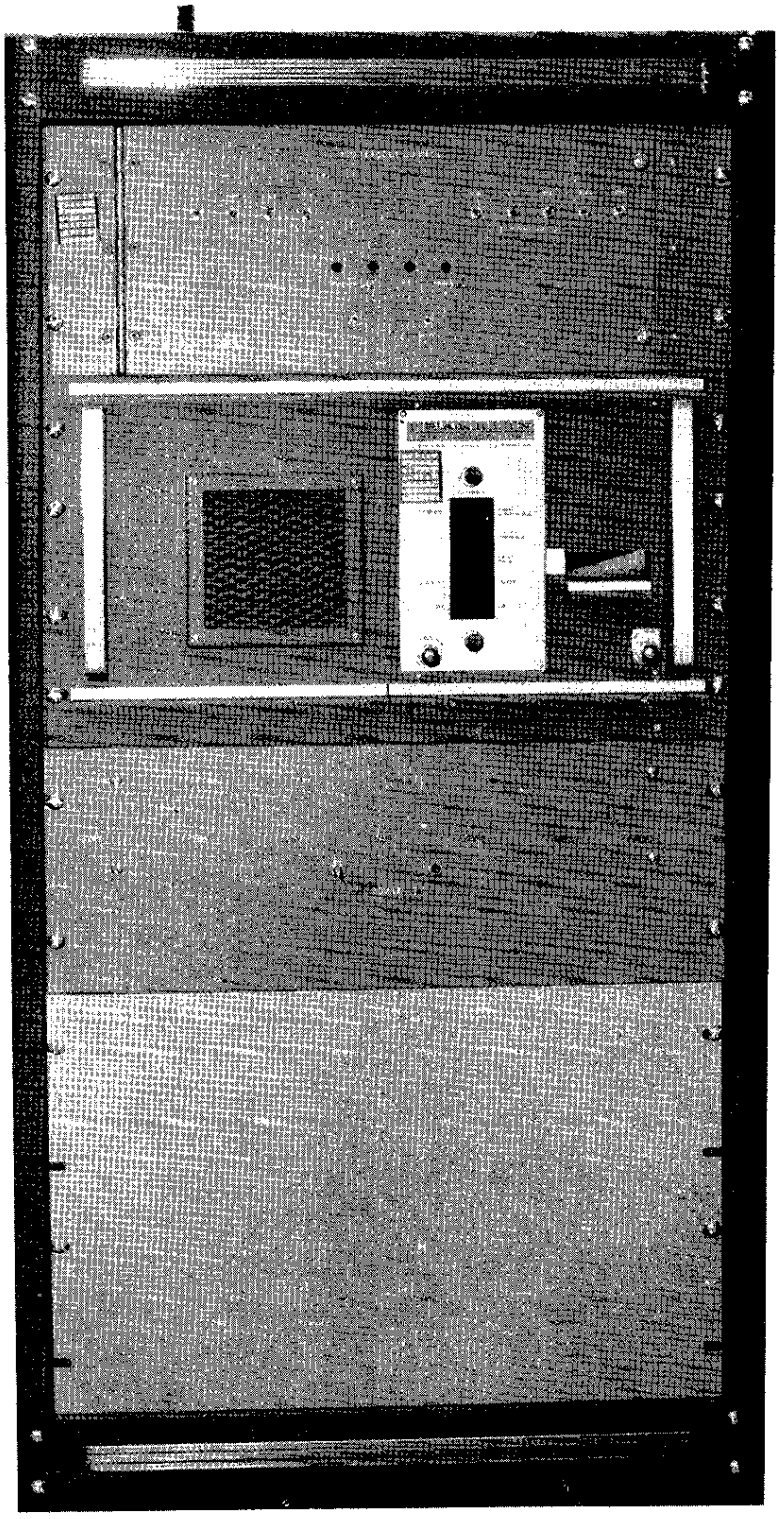

FIG. 6 DIGITAL SYSTEM

APPENDIX

DEFINITION OF TERMS AND SIGNALS

Signal	Description
START DELAY(1)	High signal, 50 μs, at beginning of each clock cycle. Provides delay for analyzer memory control operations.
EXT IRC	High signal, 1 μs, to initiate readout control of analyzer memory.
DATA ENABLE CLK	One clock pulse, low signal, gates data from analyzer memory register to 18-bit binary shift register.
SHIFT CLK	18 clock pulses to shift data from shift register through BCD converter registers.
DATA ENABLE(L)	Low signal enables parallel input data gates of 18-shift register.
SHIFT ENABLE(L)	Low signal, enables shift gates of 18-bit shift register.
PRINT COMMAND	Provides signal for printing one line on printer.
PRINTING	High signal when printer is printing a line.
STEP AB	Pulse to step BCD address register after each clock cycle.
END SCAN(L)	Low signal, at the end of 4,095th clock cycle.
RESET	Resets all registers after END SCAN(L) occurs and with a manual pushbutton.
PRINT(1)	High signal when PRINT flip-flop is set to print.
PRINT(Ø)	High signal when PRINT flip-flop is reset to not print.